Technical School of Engineering and Sciences

Public University of Navarre

DESIGN AND CONTROL OF A NEW SINGLE-SWITCH TWO-INPUT DC/DC BUCK CONVERTER FOR DUAL MPPT IN PHOTOVOLTAIC SYSTEMS

Degree in Industrial Engineering

Department of Electrical and Electronic Engineering

FINAL DEGREE PROJECT

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ABSTRACT

In the last few years, photovoltaic generation has developed very much due to an exponential reduction of market price for photovoltaic technology. The world tendency leads to medium and high-power grid-connected photovoltaic systems, as bigger systems permit to achieve better economical profitability.

This study will focus on those medium-power grid-connected photovoltaic systems, which generally use a single-stage three-phase inverter to inject power into the grid. As a result, only one maximum power point tracking (MPPT) is performed for the whole photovoltaic field, which differ from the maximum power point of each module. However, in many situations, two or more MPPTs are required in order to maximize the amount of energy produced. This is very common in residential or industrial areas, where modules usually have different inclinations or shade conditions due to the morphology of the roofs. At the moment, in those cases, there is no other choice than adding a DC/DC stage with as many DC/DC Boost converters as MPPTs are wanted. As a consequence, the conversion efficiency is reduced significantly while costs increase.

This final degree project proposes to include a new DC/DC Two-Input Buck converter in the DC/DC stage, so that the MPPT of two photovoltaic strings can be carried out at the same time using just one active switch, reducing the costs of the system. Furthermore, in this converter the semiconductors and the inductor support lower voltages, thus very high efficiency rates can be achieved.

In this work, the design and control of the Two-Input Buck converter is developed for this application, making it possible to achieve dual MPPT, high control dynamics and high efficiency.

Finally, the theoretical results previously studied will be validated by simulations.

KEYWORDS: Photovoltaic Converter, DC/DC Converter, Power Electronics, Dual Maximum Power Point Tracking, Control System Design, Nonlinearities, Small-Signal Analysis.

RESUMEN

En los últimos años, la producción de electricidad con energía fotovoltaica ha aumentado muchísimo debido a la reducción exponencial de precios que ha experimentado dicha tecnología en el mercado. La tendencia global apunta a sistemas fotovoltaicos de media y gran potencia conectadas a la red eléctrica, donde se pueden alcanzar mayores rentabilidades económicas.

Este estudio se centra en sistemas fotovoltaicos de media potencia conectados a red, que generalmente utilizan un inversor reductor trifásico para inyectar potencia a la misma. Como consecuencia, solo es posible realizar el seguimiento del punto de máxima potencia (MPPT) de todo el campo de módulos fotovoltaicos, que discierne del punto de máxima potencia de cada uno de los módulos. Este hecho supone una limitación en sistemas donde maximizar la energía producida mediante dos o más MPPT es el objetivo. Es el caso típico de zonas residenciales e industriales, donde la morfología de los tejados hace que se tengan distintas inclinaciones o sombreados para distintas partes de la instalación. Actualmente, para esas situaciones, no existe otra solución que añadir una etapa DC/DC que disponga de tantos convertidores DC/DC elevadores como MPPTs se quieren realizar. Sin embargo, ello produce una pérdida de eficiencia importante, a la vez que aumenta el coste de la instalación.

Este trabajo final de grado propone incorporar en dicha etapa DC/DC un nuevo convertidor capaz de realizar doble seguimiento del punto de máxima potencia utilizando un solo interruptor de potencia, reduciendo el coste del sistema. Además, en este convertidor, los semiconductores y la bobina soportan tensiones mucho menores, posibilitando alcanzar eficiencias muy altas.

En concreto, este proyecto se centra en el diseño y control del nuevo convertidor denominado “Two-Input Buck” o “TIBuck” para las mencionadas aplicaciones, demostrando su capacidad de realizar doble MPPT de manera rápida, eficaz, y con una eficiencia muy alta.

Para finalizar, se realizará una verificación de los resultados obtenidos teóricamente mediante sendas simulaciones.

PALABRAS CLAVE: Convertidor Fotovoltaico, Convertidor DC/DC, Electrónica de Potencia, Doble Seguimiento del Punto de Máxima Potencia, Diseño de Controladores, No Linealidades, Análisis en Pequeña Señal.

TABLE OF CONTENTS

FIGURES

TABLES

1. INTRODUCTION

1.1 Photovoltaic Energy Situation

There has been a rising awareness worldwide that renewable energy and energy efficiency are critical not only for preventing climate change, but also for the energy independence that it provides and the social profits that it offers in developing countries where energy access is regarded as a privilege.

In the last decade, a rapid growth in renewable capacity has taken place in the power sector and was dominated by two technologies: wind and solar photovoltaic. In developing countries, distributed renewable energy systems offer a great opportunity to accelerate the creation of their electrical systems, and thus to increase energy access for their inhabitants, with all the benefits that it implies. In that context, the falling costs of solar photovoltaic have made the technology the most affordable source of power for off-grid applications [1]. In figure 1.1 can be observed the quick reductive tendency of the price of crystalline silicon photovoltaic cells along the end of 20th century and the beginning of the 21st, well-known as Swanson effect. Figure 1.2 provides updated prices for crystalline photovoltaic cells in different regions of the world, showing the continuity of the reductive tendency observed in figure 1.1.

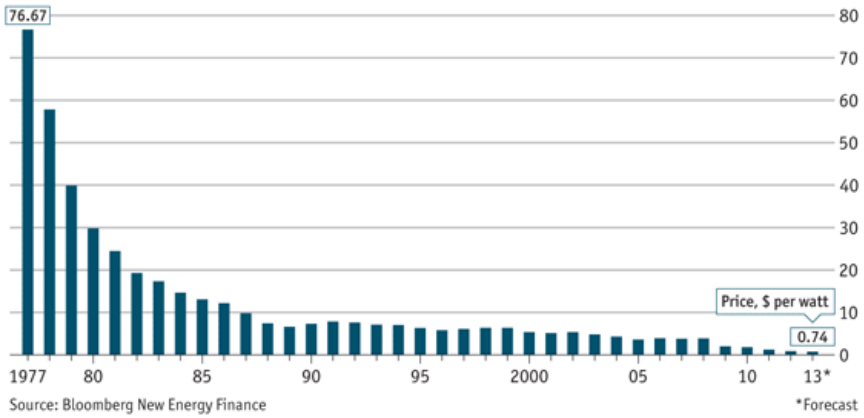

Figure 1.1. Price of crystalline silicon photovoltaic cells, $ per watt [2].

Module type, origin	€ / Wp		Trend since 2016-02		Trend since 2016-01
Crystalline modules					
Germany, Europe	0.57		- 1.7%		- 3.4%
Japan, Korea	0.63		- 3.1%		- 4.5%
China	0.55		0.0%		- 1.8%
Southeast Asia, Taiwan	0.49		0.0%		+ 2.1%

Figure 1.2. Price of crystalline silicon photovoltaic cells, March 2016 [3].

Solar photovoltaic is starting to play a substantial role in electricity generation in some countries, as fast falling costs have made unsubsidised solar photovoltaic energy cost-competitive compared to fossil fuels, even though oil and natural gas prices have dropped as well. In 2015, solar photovoltaic marked another record year in growth, with an estimated 50 GW installed for a total global capacity of about 227 GW, as observed in figure 1.3.

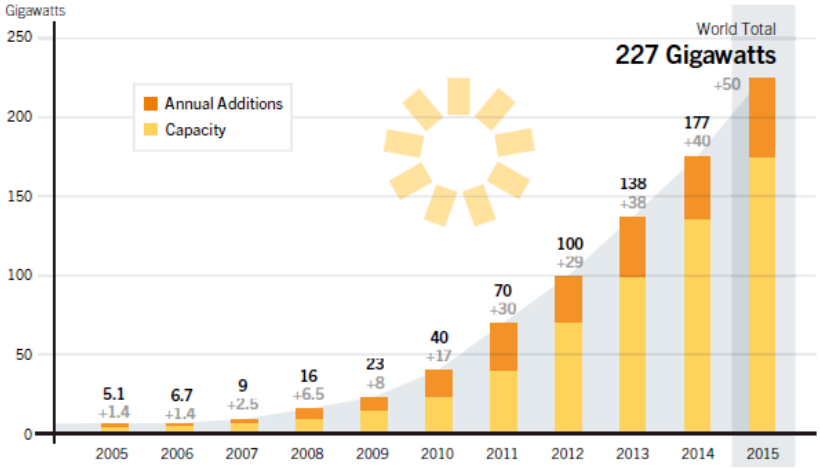

Figure 1.3. Photovoltaic total capacity in the world, 2015 [1].

China, Japan and the United States accumulated the vast majority of the new capacity. Even so, the distribution of new installations continued to spread out in Latin America, Middle East and in several African countries. Broadly speaking, European markets picked up after three years of decline, while China became the first country to overtake Germany in the world ranking of total solar photovoltaic capacity [1].

In the last few years, consolidation among manufacturers continued, as new cell and module facilities have opened around the world, in order to meet the rising demand. This produced an on-going regional shift of renewable energy sector workers from Europe and North America to China and other Asian nations, due to its undisputed lead in manufacturing as well as their rapid expanding domestic markets [1]. In 2015 an estimated 8.1 million people worked directly or indirectly in the sector, with an additional 1.3 million in large-scale hydropower, as represented in figure 1.4.

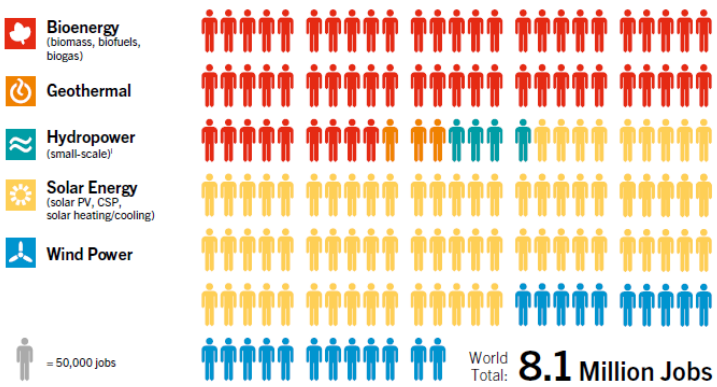

Figure 1.4. Jobs in renewable energy [1].

Solar photovoltaic is the largest employer of all technologies with 2.8 million jobs, most of which are still concentrated in China. Japan, the United States, and India have also increased their solar photovoltaic employment, while in Europe photovoltaic industry continued dropping more than a 35% since 2013 [1].

1.2 DC/DC Power Converters

DC/DC converters are commuted circuits that make it possible to transform a DC voltage into another DC voltage of a different value. Generally, the input voltage of the converter is a non-regulated voltage source (rectification of the grid, battery, etc.) while the output is a regulated voltage. This is possible because the duty cycle (D) of the switches can be controlled to obtain the desired voltage at the output. This is why DC/DC converters are typically used as adjustable voltage sources, for example in motor applications.

Power converters use semiconductors as power switches, which can be controlled or non-controlled. Controlled semiconductors are those which can be switched on and/or off with freedom (Tiristor, BJT, Mosfet, IGBT..), and non-controlled semiconductors are those which switch on/off depending on the electrical conditions of the circuit (Diodes). Regardless of the type of switches used, they have to be complementary. This means that when one of them is on, the other has to be off and the other way round, so that short circuits or open circuits never take place.

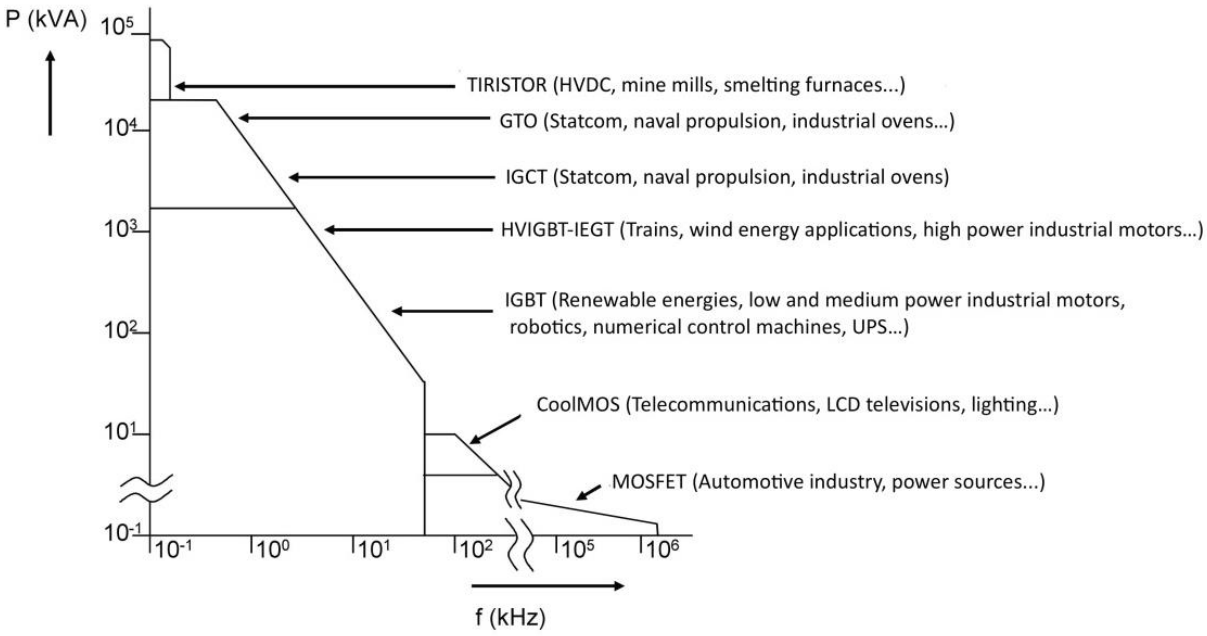

Figure 1.5. Typical semiconductors and applications [4].

The electrical structure of the power converter defines the limits between which the output voltage can be regulated with de duty cycle. Therefore, one can distinguish different topologies of DC/DC power converters. These are the most typical ones:

- Buck converter. With a voltage source at the input and a current source at the output, it can supply an output voltage equal or lower than the input.

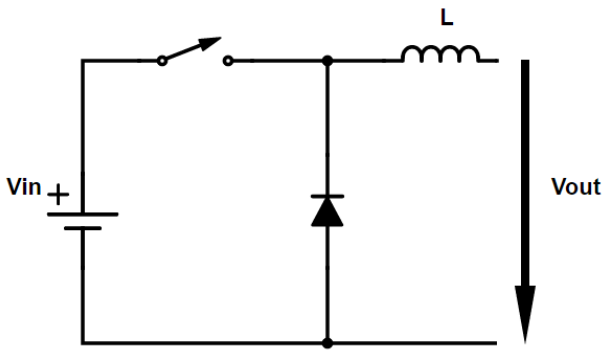

Figure 1.6. Buck converter.

$$V_{out}=V_{in} \cdot D$$

- Boost converter. With a current source at the input, and a voltage source at the output, it can supply an output voltage equal or higher than the input.

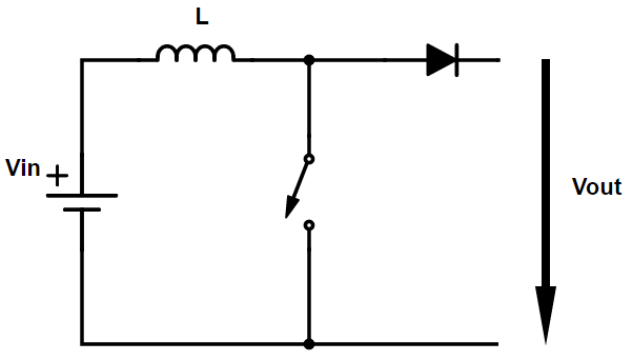

Figure 1.7. Boost converter.

$$V_{out} = \frac{V_{in}}{(1 - D)}$$

- Buck/Boost converter. It is a mix of the two previous configurations, and it can supply an output voltage lower, equal or higher than the input.

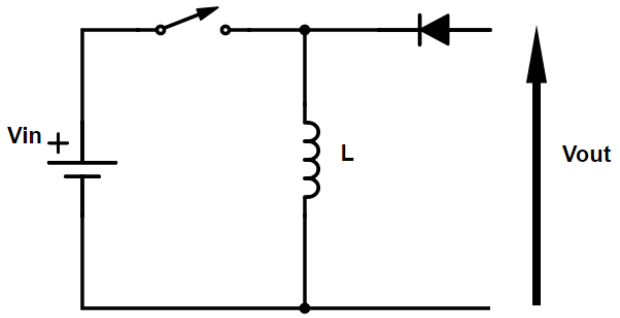

Figure 1.8. Buck/Boost converter.

$$V_{out} = V_{in} \frac{D}{(1 - D)}$$

Depending on the application, all these types of converter topologies can be easily redesigned to work with one-way flux energy, if the output of the converter is a pure load, or to be power reversible, if the load can sometimes generate energy and the input of the converter can consume it.

1.3 Medium-Power Grid-Connected Photovoltaic Systems

The target of this project are medium-power grid-connected photovoltaic systems, between 10 kW and 100 kW, where the number of photovoltaic modules makes it possible to reach the high voltage needed in the DC bus of the three-phase inverter. This scenario is common in many countries, especially in European ones, which are betting high with configurations like the ones shown in the next figures:

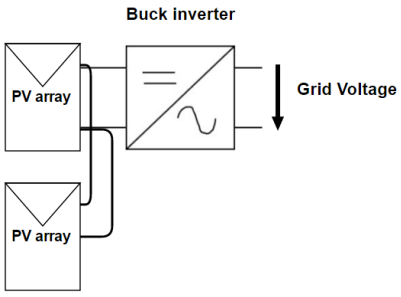

Figure 1.9. Single AC/DC stage.

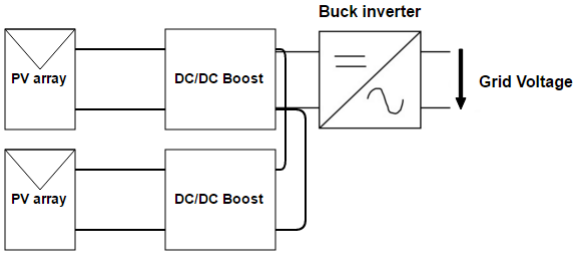

Figure 1.10. AC/DC & DC/DC stage using two parallel Boost converters.

Figure 1.9 shows a configuration with a single AC/DC stage, composed by two strings of photovoltaic modules directly connected to a three-phase inverter.

In this system, only one MPPT is performed for the whole photovoltaic field, so the working point of the photovoltaic modules could be inefficient or at least less efficient than wanted.

On the other hand, figure 1.10 represents the only choice available when dual MPPT is required. This configuration makes use of a DC/DC stage performed by two parallel Boost converters, followed by an AC/DC stage using a three-phase inverter. In this situation, dual MPPT can be performed (one MPPT with each DC/DC Boost converter), making it possible to optimize the amount of energy extracted. However, the efficiency and costs of the system are harmed by the added DC/DC stage.

The new DC/DC Two-Input Buck converter proposed can perform dual MPPT with only one active switch, which is a real advantage in terms of costs, as it means that the converter can do the same task than two parallel Boost using half the number of semiconductors. Furthermore, the semiconductors and the inductor support lower voltages, making it possible to achieve efficiencies over 99.85% using an inductor 16 times smaller than each Boost in figure 1.10. The result is a much more optimal solution to the problem.

The proposal is to add a DC/DC stage using the Two-Input Buck converter in Figure 1.9, and to substitute the two DC/DC Boost converters with just one Two-Input Buck converter in Figure 1.10, as represented in the next figure 1.11:

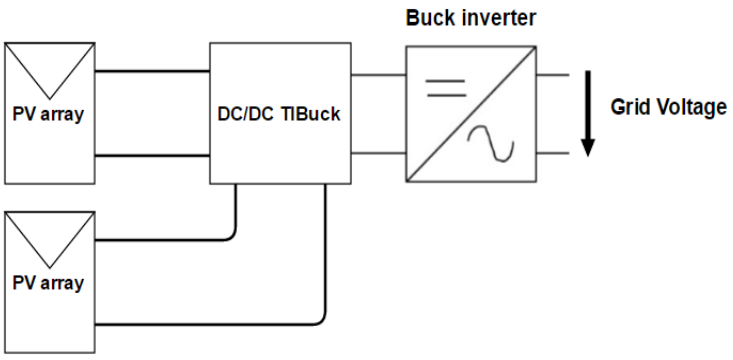

Figure 1.11. Proposed configuration using the new TIBuck converter.

The dual MPPT capability of the TIBuck converter makes very interesting the possibility of integrating the proposed configurations in industrial areas with different photovoltaic technologies, or different conditions due to the morphology of the roofs like inclination, shades or temperature, as typical examples.

2. BUCK CONVERTER

From this point forward it will explained, more in depth, how do Buck converters operate, since this is the most similar configuration to the new converter.

2.1 Overview

As it has been explained in the introduction, Buck converters provide a regulated below-input voltage at the output. The degree of freedom is the duty cycle of the controlled switch, which allows managing the output voltage. That is the typical purpose of the converter.

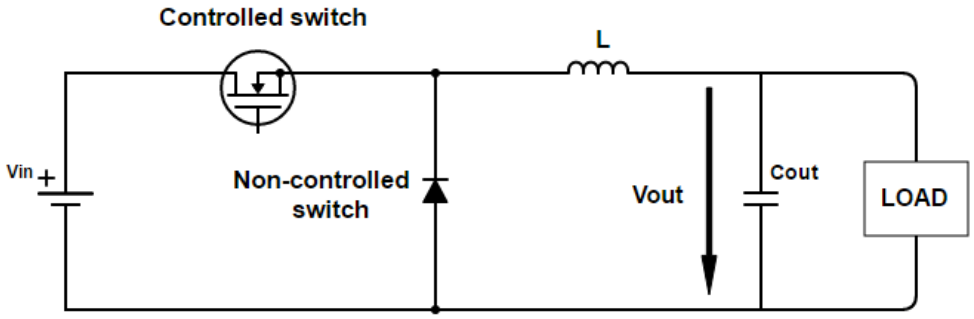

Figure 2.1. Buck converter.

As figure 2.1 shows, there are two types of semiconductors. There is a controlled switch, which is usually a MOSFET or an IGBT depending on the power requirements of the application, and a non-controlled switch, which is normally a diode.

The Buck converter has two conduction modes, depending on the behaviour of the inductor current:

- **Continuous Conduction Mode (CCM).** The inductor current never gets to zero. It is the most common situation.

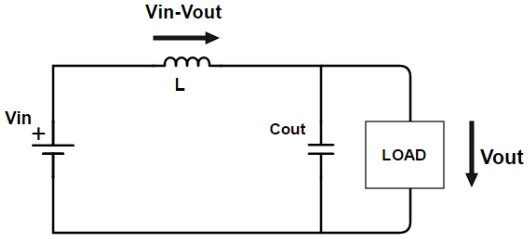

Figure 2.2. Controlled switch is on.

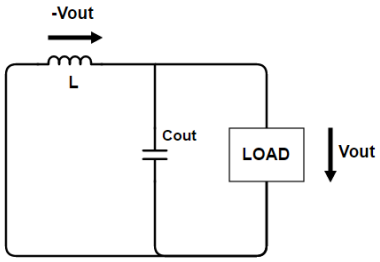

Figure 2.3. Controlled switch is off.

When the controlled switch is on, the inductor has a positive voltage that makes the current increase, and so the voltage at the load. When the controlled switch is off, the current of the inductor switches on the diode and the voltage at the inductor changes to be $-V_{out}$. This makes de current decrease, and so the voltage at the load. The output voltage is related with the input voltage through the duty cycle as shown in expression 2.1:

$$V_{out}=V_{in}\cdot D \tag{2.1}$$

- **Discontinuous Conduction Mode (DCM).** The inductor current gets to zero some when in the operation time, typically due to a small current required by the load combined with a relative high ripple.

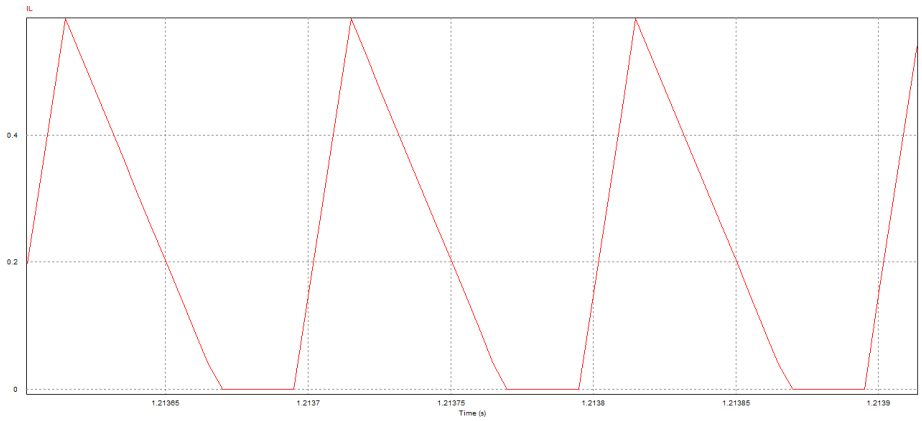

Figure 2.4. Inductor current in CDCM.

During the period when the controlled switch is off, the current falls down faster than $(1-D)\cdot T_{com}$ (Where T_{com} is the commutation period) and that makes the current get to zero or below zero. If the converter is power-reversible, then the current will turn negative and the output capacitor will discharge.

If it is not reversible the current establishes at zero, both the controlled and the non-controlled switches are off, and the equations of the converter change. In this case, the output voltage of the converter depends not only on the duty cycle (D) and the input voltage (V_{in}), but also on the average inductor current ($<i_L>$), the inductance (L) and the commutation frequency (F_{com}).

$$V_{out}=\frac{V_{in}}{\frac{<i_L>\cdot 2\cdot L\cdot F_{com}}{D^2\cdot V_{in}}+1} \tag{2.2}$$

2.2 Design of the Buck Converter

There are four main elements that have to be designed in the Buck converter: The two semiconductors, the inductor, and the output capacitor. To properly optimize the design, the worst electrical conditions for each of them have to be analysed.

- **The controlled switch.** To choose the correct type and model of switch, it is required to measure the voltage and current that will manage the semiconductor in steady-state operation.

  · When it is on, it is managing all the inductor current, the steady state value of which is I= $\frac{V_{out}}{R_{load}}$, if connected to a pure resistance.

  · When it is off, the diode is on and therefore the voltage of the switch is V_{in}.

- **The non-controlled switch.** A similar analysis is carried out with the diode:

  · When it is on, it is managing again all the inductor current I= $\frac{V_{out}}{R_{load}}$ if connected to a pure resistance.

  · When it is off, the controlled switch is on and the voltage suffered by the diode is V_{in}.

- **The inductor.** The inductance value has a direct effect on the inductor current ripple. The bigger the inductor is, the lower the current ripple will be. As a result, a maximum desirable current ripple (Δi_L) must be set up by the designer for the worst situation (D=0.5). The expression which relates both values is:

$$L=\frac{V_{in}}{4\cdot F_{com}\cdot \Delta i_L} \tag{2.3}$$

  Where V_{in} is the input voltage, and F_{com} the commutation frequency.

- **The capacitor.** There are many strategies to choose the capacitor value, but in this case just one of them is used. The capacitor size has a direct effect on the output voltage ripple, in other words, in its stability.

As the inductor and the output capacitor make up a low-pass filter, and the output voltage of the converter is a commuted signal, once the inductor value is established the capacitor size can be determined depending on how much it is wanted to filter the output voltage. The expression that relates those values is:

$$C = \frac{1}{(2 \cdot \pi \cdot F_{filter})^2 \cdot L} \quad (2.4)$$

Where F_{filter} is the cut-off frequency of the filter, and L the inductance value.

2.3 Control of the Buck Converter

2.3.1 Control of the output voltage

The control of the converter is a key part when designing it. The performance of the system depends on the control, and the same controls are not acceptable for all the applications.

As a consequence, different strategies must be studied depending on the purpose of the converter. In the vast majority of them, a proportional and integral regulator (PI) with the corresponding compensations is sufficient to control the dynamic of this converter. The proportional part provides with rapid response, while the integral part allows eliminating steady-state error, giving stability to the control.

Single-loop or cascaded-loop structures can be developed to control Buck converters, as shown in the following figures:

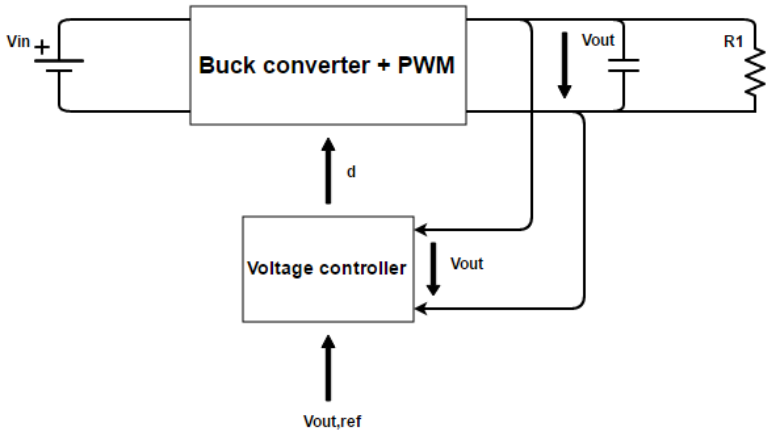

Figure 2.5. Control of the output voltage with a single loop.

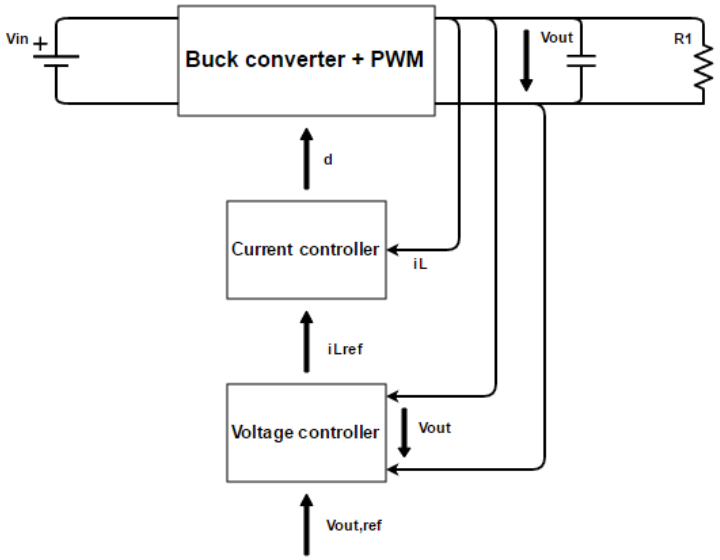

Figure 2.6. Control of the output voltage with cascaded-loops.

In figure 2.5, the single control loop calculates directly the duty cycle needed to have the voltage reference at the output, with no control of the inductor current.

Normally, cascaded-loop structures with an inner current loop and an outer voltage loop are preferred (figure 2.6), since the current at the inductor (which the semiconductors have to manage) can be controlled and limited, making the system a lot more reliable.

2.3.2 Control of the input voltage

Nevertheless, a more realistic analogy with this project would be to use the degree of freedom (duty cycle D) to modify the input voltage of the converter (photovoltaic array voltage), while the output being the “non-regulated”, or more precisely externally-regulated voltage source, as it is controlled by the DC bus voltage controller of the inverter.

A different point of view must be considered in the control strategy, but a cascaded-loop structure is still the best option due to the same arguments previously mentioned. In this case, the cascaded loop structure changes are represented in figure 2.7.

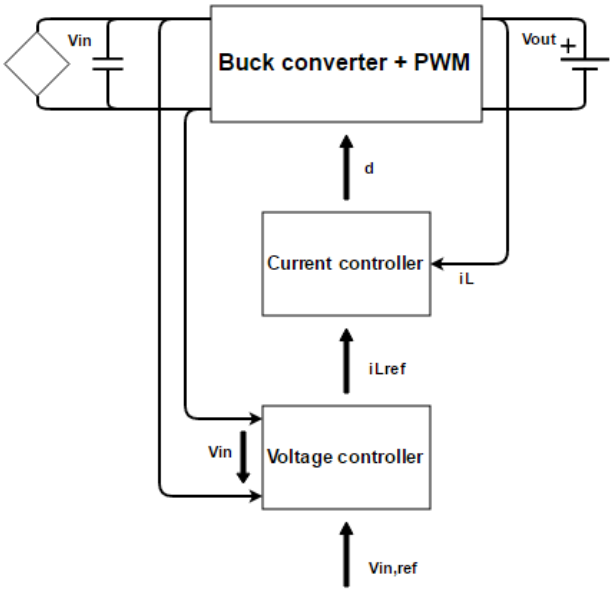

Figure 2.7. Control of the input voltage, cascaded-loop.

It can be observed that the inner current loop remains unchanged, while the outer voltage loop changes as does the purpose of the control, which now focuses on the input voltage.

2.3.2.1 Inner current loop

With this inner loop, the inductor current is intended to be controlled with the duty cycle of the controlled switch (d). Therefore, it is needed to determine the transfer function of the system that relates both parameters G= $\frac{i_L}{d}$, as represented in figure 2.8:

Figure 2.8. Schematic of the plant of the system.

The voltage at the inductor is v_L=$L\frac{di_L}{dt}$, and when applying the Laplace transformation one obtains that $V_L = L \cdot s \cdot I_L(s)$.

As it has been explained, in continuous conduction mode (CCM) the mean voltage at the inductor during one commutation period is $V_L=V_{in} \cdot D - V_{out}$. Combining both expressions, one gets:

$$I_L = \frac{V_{in} \cdot D - V_{out}}{Ls} \quad (2.5)$$

Therefore, the transfer function of the system has been determined, and the proportional and integral controller (PI) can be designed to control the system, using appropriate compensations:

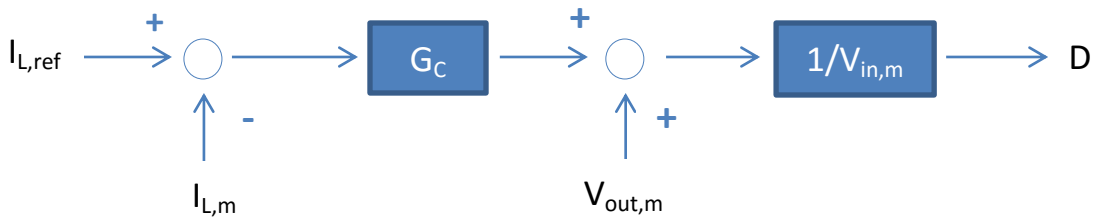

Figure 2.9. Scheme of the inner current loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference, D the duty cycle of the controlled switch, and $I_{L,m}$, $V_{out,m}$ and $V_{in,m}$ the inductor current, the output voltage, and the input voltage measurements respectively.

In this case, the control requirements were set up us follows:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	500 Hz
Phase margin	60º

Table 2.1. Parameters to design the controller #1.

And the PI controller needed with the mentioned requirements results

$$G_C = \frac{1.687 \cdot (0.002456s + 1)}{0.002456s}$$

2.3.2.2 External voltage loop

A similar strategy is carried out with this outer loop. Now, the relationship between the inductor current and the input voltage $G = \frac{v_{in}}{i_L}$ has to be determined.

Figure 2.10. Schematic of the plant of the system.

Figure 2.10 shows the plant that needs to be determined. In this case, the input capacitor that stabilizes the photovoltaic array voltage has to be analysed. The photovoltaic array model is considered as a pure current source, although a shunt resistance should be taken into account if a precise study is wanted to be made. As this is not the purpose of this chapter, a simple current source (I_{in}) is enough to show the philosophy of the methodology. This model is represented in figure 2.11:

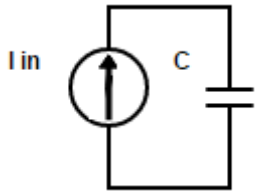

Figure 2.11. Simplified model of the photovoltaic string.

The current at the input capacitor is $i_c = C\frac{dv_{in}}{dt}$, and applying the Laplace transformation one obtains that $I_C=C\cdot s\cdot V_{in}$.

If the Kirchhoff Current Law is applied to the input capacitor, then the second expression needed is obtained: $i_C = i_{in} - i_L \cdot d$. Combining both equations, and applying the Laplace transformation, the result is:

$$V_{in}=\frac{I_{in}-I_L\cdot D}{Cs} \qquad (2.6)$$

The transfer function of the system has been again determined, and to control it a proportional and integral controller (PI) with compensations can be used, shown in figure 2.12:

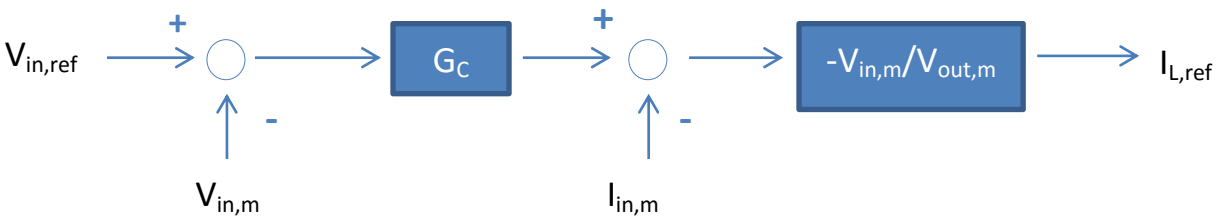

Figure 2.12. Scheme of the external voltage loop.

Where G_C represents the PI controller, $V_{in,ref}$ the input voltage reference, $I_{L,ref}$ the inductor current reference, and $I_{in,m}$, $V_{out,m}$ and $V_{in,m}$ the photovoltaic current, the output voltage, and the input voltage measurements respectively.

In order to calculate de PI controller, it is recommended to take into account the inner current loop as a first-order transfer function with a pole at the loop cut-off frequency $\frac{1}{\frac{1}{2\pi 500}s+1}$. The rest of the parameters are set up as represented in table 2.2:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	50 Hz
Phase margin	60º

Table 2.2. Parameters to design the controller #2.

It can be noticed that the cut-off frequency of the external loop is set 10 times lower than the inner current loop, to ensure they are decoupled.

With those specifications, the PI controller needed is $G_C = \frac{0.0237 \cdot (0.007916s+1)}{0.007916s}$

3. NEW TWO-INPUT BUCK CONVERTER

Actually, this Two-Input Buck converter was first proposed in [5] by J.Sebastian, P.J. Villegas, F. Nuno, and M.M. Hernando, but with a very different perspective since it was conceived as a postregulator, where all the attention is paid to the output voltage. 20 year later, this project will take advantage of the benefits of this converter to create an unprecedented conversion topology for photovoltaic systems, where a completely different point of view is needed.

3.1 Converter Overview

The new converter proposed in this project is shown in figure 3.1. It has two power inputs (V_1 and V_2) , which represent the two photovoltaic strings, and one power output that represent the DC bus of the three-phase inverter (V_o) . From now on it will be called just TIBuck.

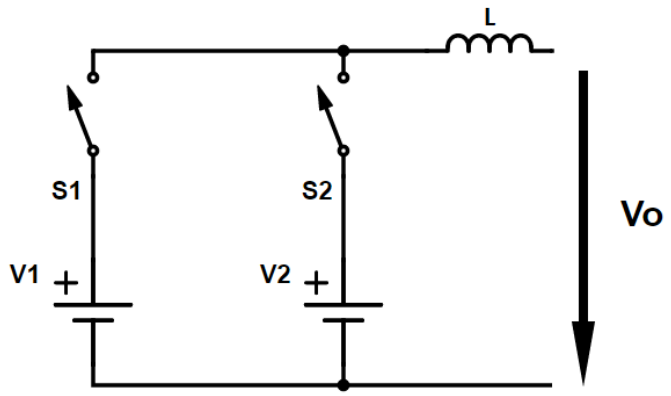

Figure 3.1. TIBuck model with voltage sources.

The similarities with the classic Buck structure described in chapter 1.2 can be easily appreciated, although the semiconductors are not specified yet.

In this first analysis, the two power inputs will be considered as voltage sources. There is no need to specify the kind of semiconductors yet, just to take into account that they are complementary. Power reversible situations will be not considered either.

With just having a look at the figure, one can notice big similarities with the Buck converter, although the topology of this converter cannot be determined as pure reducer yet.

With a brief analysis, one can notice how the converter works:

- When switch S1 is on, S2 is off and the inductor voltage is V_1-V_{out}.
- When switch S1 is off, S2 is on and the inductor voltage is V_2-V_{out}.

It is well known that the mean inductor voltage in a commutation period in steady-state operation has to be zero. Therefore, it is easy to see that $V_1>V_{out}>V_2$, the other way round $V_2>V_{out}>V_1$, or $V_1=V_{out}=V_2$ in order to accomplish that condition. As a consequence, the converter performs as a Buck for one input and as a Boost for the other one.

If $V_1>V_{out}>V_2$ then the switch S1 has to support positive voltage (V_1-V_2) and positive current ($<i_L>$) and S2 has to support positive voltage (V_1-V_2) and negative current ($-<i_L>$) , considering the references as in figure 3.2:

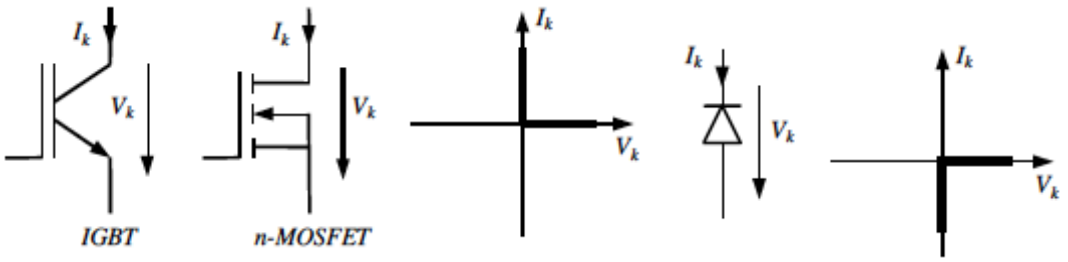

Figure 3.2. Segment analysis for different semiconductors. [5]

Therefore, S1 has to be a controlled switch (not determined if MOSFET or IGBT) and S2 a non-controlled switch, typically a diode.

If $V_2>V_{out}>V_1$ then the switch S2 has to support positive voltage and current and S1 negative voltage and current, with the same references of the figures above. As a consequence, S2 has to be a controlled switch (Not determined if MOSFET or IGBT) and S1 a non-controlled switch, typically a diode.

Depending on the input sources nature, if both conditions are required to be satisfied, then switches that support positive and negative voltages would be necessary, but the current will go only from the photovoltaic panel to the load. Thus, it could be for example a MOSFET or IGBT with a series diode.

It is senseless to consider the situation $V_1=V_{out}=V_2$ to determine the semiconductors of this converter, as none of them would be necessary.

However, it is clear that the output voltage of the converter has to be between the input voltages. It will be considered that S1 and S2 are controlled switches, where D is the part of time that the switch S1 is connected. From the mean voltage at the inductor, one can get the output voltage expression of the converter:

$$V_{out}=V_2+(V_1-V_2)\cdot d \quad (3.1)$$

When analysing the voltage and current stress suffered by the semiconductors, one appreciates that are the same for both switches:

$$V_{S1}=V_{S2}=V_1-V_2 \quad (3.2)$$

$$I_{S1}=I_{S2}=\langle i_L\rangle=\frac{V_{out}}{R_{load}} \text{ when connected to a pure resistance} \quad (3.3)$$

Notice that the more equal the both input voltages are, the less voltage stress the switches suffer, which is a critical value for them. Actually, the switches cannot be determined before quantifying the voltage they have to support.

The distribution of the photovoltaic modules is up to the designer, and as the modules will typically operate near the MPP in both strings, that value can be really low if similar series modules are situated in both inputs, reducing significantly the losses of the converter.

In that situation, V_1-V_2 would be a low value, and V_{out} would be even a closer value to both of them. That means that the voltages at the inductor V_1-V_{out} and V_2-V_{out} during the commutation would be low as well, so that smaller inductance would be necessary for the same current ripple obtained in an equivalent Buck converter.

3.2 Steady State Analysis

In this analysis, the different conduction modes of this converter will be studied, and the expressions that determine its behaviour in each case will be calculated. For this deeper analysis, the photovoltaic arrays will be considered as current sources with input capacitors instead of simple voltage sources, but for the moment without the shunt resistance of the real photovoltaic model, as it is not relevant for understanding how the converter works. As shown in figure 3.3, in this project only S1 will be considered as a controlled switch, so that $V_1 \geq V_{out} \geq V_2$.

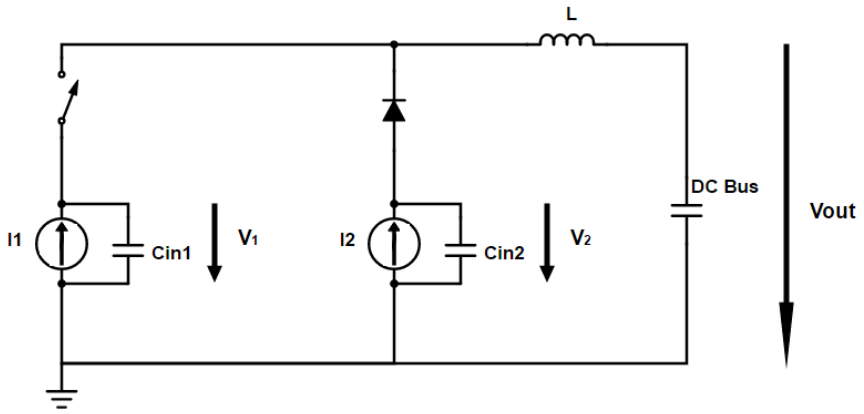

Figure 3.3. TIBuck model with current sources and parallel capacitors

The three main equations that represent the dynamic of the system involve the two input capacitors and the inductance, and are exposed in the next lines:

$$L\frac{di_L}{dt} = v_1 \cdot d + v_2 \cdot (1-d) - v_{out} \quad (3.4)$$

$$C\frac{dv_1}{dt} = i_1 - i_L \cdot d \quad (3.5)$$

$$C\frac{dv_2}{dt} = i_2 - i_L \cdot (1-d) \quad (3.6)$$

And out of them will be obtained the steady-state equations, as well as other required in different parts of the project.

3.2.1 Continuous conduction mode (CCM)

The first expressions of the converter have already been obtained for continuous conduction mode (CCM):

· Output voltage of the converter: $V_{out}=V_2+(V_1-V_2)\cdot D$ (3.7)

· Voltage and current stress of the converter switches: $V_{switches}=V_1-V_2$ and $I_{switches}=\langle i_L \rangle$ (3.8)

As voltages sources have been replaced with current sources and input capacitors, new equations must be added:

· Mean current at the input capacitor 1 is zero. $\langle i_L \rangle = \frac{I_1}{D}$ (3.9)

· Mean current at the input capacitor 2 is zero. $\langle i_L \rangle = \frac{I_2}{1-D}$ (3.10)

Combining both expressions, one gets the expression that relates the duty cycle with the two input currents:

$$D = \frac{I_1}{I_1 + I_2} \tag{3.11}$$

Introducing this equation in all the previous ones, leads to the following expressions:

$$\langle i_L \rangle = I_1 + I_2 \tag{3.12}$$

$$V_{out} = \frac{V_1 \cdot I_1 + V_2 \cdot I_2}{\langle i_L \rangle} \tag{3.13}$$

Both equations make sense; the mean current at the inductor is the sum of the two mean currents of the switches during a commutation period (which are the photovoltaic currents, since the mean current of the input capacitors are zero), and the output voltage is a weighted mean of the input voltages with the photovoltaic currents.

3.2.2 Current discontinuous conduction mode (CDCM)

In this mode, 3 different periods will be differentiated inside one commutation period, as represented in figure 3.4:

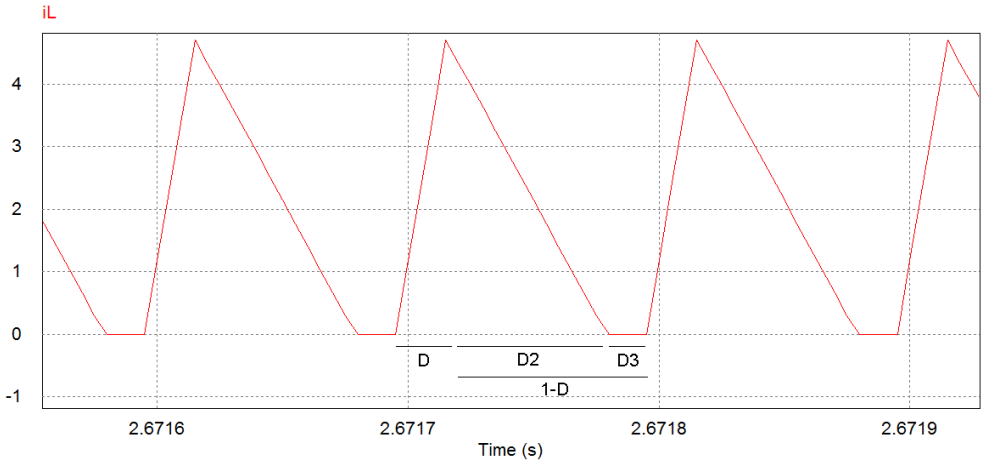

Figure 3.4. Inductor current in CDCM.

- $T_1 = D_1 \cdot T_s = D \cdot T_{com}$. It is the time that the controlled switch is on. The voltage at the inductor is positive and the current rises up.
- $T_2 = D_2 \cdot T_{com}$. It is the time the current drops until it gets to zero, while the controlled switch is off.

- $T_3 = D_3 \cdot T_{com}$. It is the time when both the controlled and the non-controlled switches are off and the current at the inductor is still zero.

In this mode, one can obtain four main equations from which the behaviour of the converter can be determined:

- i_L grows as much in T_1 as decreases in T_2:

$$D_2 = D_1 \cdot \frac{V_1 - V_{out}}{V_{out} - V_2} \rightarrow V_2 = V_{out} - \frac{D_1}{D_2} \cdot (V_1 - V_{out}) \quad (3.14)$$

- The value of the inductor current ripple Δi_L.

$$\Delta i_L = \frac{(V_1 - V_2) \cdot D_1 \cdot D_2}{L \cdot F_{com} \cdot (D_1 + D_2)} \rightarrow V_1 = V_2 + \frac{\Delta i_L \cdot (D_1 + D_2) \cdot L \cdot F_{com}}{D_1 \cdot D_2} \quad (3.15)$$

  Where F_{com} represents the commutation frequency.

- The mean current at the input capacitor one $\langle i_{C1} \rangle$ is zero.

$$D_1 = \frac{2 \cdot I_1}{\Delta i_L} \rightarrow \Delta i_L = \frac{2 \cdot I_1}{D_1} \quad (3.16)$$

- The mean current at the input capacitor two $\langle i_{C2} \rangle$ is zero.

$$D_2 = \frac{2 \cdot I_2}{\Delta i_L} \rightarrow \Delta i_L = \frac{2 \cdot I_2}{D_2} \quad (3.17)$$

Combining then, one gets the relations between the input voltages, the input currents, and the two degrees of freedom (V_{out} and D):

$$V_1 = V_{out} + \frac{2 \cdot L \cdot F_{com} \cdot I_1}{D^2} \quad (3.18)$$

$$V_2 = V_{out} - \frac{2 \cdot L \cdot F_{com} \cdot {I_1}^2}{I_2 \cdot D^2} \quad (3.19)$$

$$\langle i_L \rangle = I_1 + I_2 \quad (3.20)$$

Focusing on the control, the duty cycle and the output voltage equations depending on the desired input voltages V_1 and V_2, and with photovoltaic array currents I_1 and I_2 are:

$$D=\sqrt{\frac{2\cdot L\cdot F_{com}\cdot I_1\cdot \langle i_L\rangle}{I_2\cdot(V_1-V_2)}} \quad (3.21)$$

$$V_{out}=\frac{V_1\cdot I_1+V_2\cdot I_2}{\langle i_L\rangle} \quad (3.22)$$

Notice that the output voltage expression, and mean inductor current expressions (3.18 and 3.20) are the same than in CCM, but the duty cycle is rather complicated.

3.2.3 Voltage discontinuous conduction mode (VDCM)

This third mode is very specific for this converter. As it has two input voltages, and when working with high duty cycles, both input voltages can achieve the same value due to the voltage ripple of their capacitors, making both switches conduct at the same time. Three different periods will be again distinguished inside one commutation period, as shown in figure 3.5:

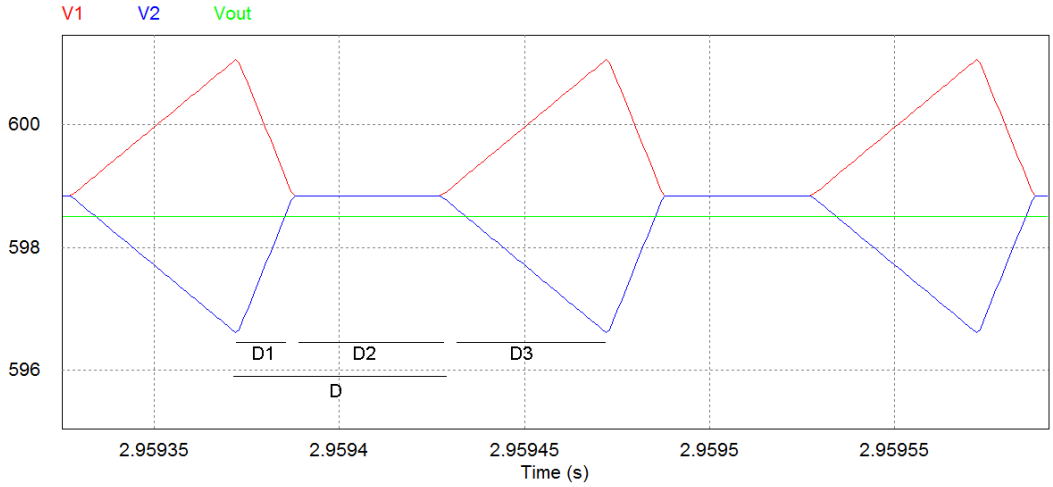

Figure 3.5. Input voltages in VDCM.

- $T_1 = D_1\cdot T_{com}$. The controlled switch is on. The voltage at the input capacitor 1 drops, while the voltage at the input capacitor 2 rises up due to the photovoltaic current source, and both voltages converge at the same value.
- $T_2 = D_2\cdot T_{com}$. $V_1=V_2=V_o$ but not necessarily equal to the output voltage V_{out}. V_1 cannot drop lower than V_2 and V_2 cannot rise up higher than V_1, and both switches are on at the same time.
- $T_3 = (1\text{-}D)\cdot T_{com}$. When the controlled switch turns off, the input capacitor 1 starts to charge again and the capacitor 2 discharges, so that V_1 rises up and V_2 drops off. In this commutation, there is no voltage stress for the semiconductors.

As there are two input voltage sources, and supposing $V_1 \geq V_{out} \geq V_2$, only one controlled switch is needed. During T_1, V_1 decreases and V_2 increases, and if both average values are very close to each other, then V_2 can achieve V_1 value and both voltages cannot change until de controlled switch turns off.

The main equations can be obtained based on a similar analysis done in the previous modes:

- Mean current at the capacitor 1 is zero. $\langle i_L \rangle = I_1 \cdot (1 + \frac{D_1}{D_3})$ (3.23)
- Mean current at the capacitor 2 is zero. $\langle i_L \rangle = I_2 \cdot (1 + \frac{D_1}{D_3})$ (3.24)

Combining then, one has again that $\langle i_L \rangle = I_1 + I_2$, as expected.
From now on, ΔV_1 and ΔV_2 will refer to the increase (positive) or decrease(negative) of V_1 and V_2 during T_1.

Then, the mean voltages $\langle V_1 \rangle$ and $\langle V_2 \rangle$ can be expressed as:

$$\langle V_1 \rangle = V_o + \frac{\Delta V_1}{2} (D_1 + D_3) \quad (3.25)$$

$$\langle V_2 \rangle = V_o - \frac{\Delta V_2}{2} (D_1 + D_3) \quad (3.26)$$

As $|\Delta V_1| = |\Delta V_2|$, similar expressions are obtained in both cases:

$$\langle V_1 \rangle = V_o + \frac{I_1 \cdot \langle i_L \rangle \cdot (1-D)^2}{2 \cdot I_2 \cdot C_1 \cdot F_{com}} \quad (3.27)$$

$$\langle V_2 \rangle = V_o - \frac{I_1 \cdot \langle i_L \rangle \cdot (1-D)^2}{2 \cdot I_2 \cdot C_1 \cdot F_{com}} \quad (3.28)$$

Where F_{com} represents the commutation frequency.

Combining them, and focusing on the control, one gets that:

$$D = 1 - \sqrt{\frac{(V_1 - V_2) \cdot I_2 \cdot C_1 \cdot F_{com}}{I_1 \cdot \langle i_L \rangle}} \quad (3.29)$$

Analysing the voltage at the inductor, and keeping in mind that the mean voltage has to be zero, one obtains the same output voltage expression than in the other conduction modes:

$$V_{out}= \frac{V_1 \cdot I_1 + V_2 \cdot I_2}{\langle i_L \rangle} \quad (3.30)$$

Having expressed the two degrees of freedom with the circuit parameters, now the input voltages equations can be written clearly:

$$\langle V_1 \rangle = V_{out} + \frac{I_1 \cdot (1-D)^2}{C_1 \cdot F_{com}} \quad (3.31)$$

$$\langle V_2 \rangle = V_{out} - \frac{{I_1}^2 \cdot (1-D)^2}{I_2 \cdot C_1 \cdot F_{com}} \quad (3.32)$$

The current ripple can also be expressed in terms of photovoltaic currents and the duty cycle:

$$\Delta i_L = \frac{{I_1}^2 \cdot (1-D)^2}{(I_1+I_2) \cdot L \cdot C \cdot F_{com}} \quad (3.33)$$

This conduction mode has very interesting consequences derived from the proximity of V_1, V_2 and V_{out} values:

1- Both switches support low voltage stress V_1-V_2, and therefore the losses are very low. In addition, when switch S1 turns off and switch S2 turns on, both commute with voltage stress zero, which means that there are no losses.
2- The inductor support low voltage stress as well, and consequently the current ripple is very small.
3- The time that the input voltages V_1 and V_2 are constant, makes the voltage ripple smaller than in the other modes. If the duty cycle increases, the time that the input voltages are constant increases and the voltage ripple at the capacitors diminishes.

With all these advantages, it may be interesting to work in this mode if the desired MPP voltages at the two photovoltaic strings are very close. This situation can happen if a similar number of photovoltaic modules is located in both strings.

3.2.4 Conduction mode dependent on the desired voltages

The MPPT algorithm calculates de string voltages necessary to maximize the energy generated by the photovoltaic modules. Depending on how close are those values, the TIBuck converter must work in one mode or another. As seen before, the converter equations change drastically from one mode to another, so it is essential to determine

how must the converter work at any time to achieve the MPPT voltages in both photovoltaic strings.

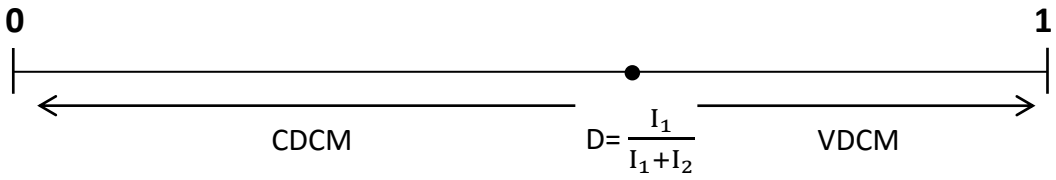

Figure 3.6. Duty cycle for each conduction mode.

Figure 3.6 represents the duty cycle that makes the converter work in each mode depending on the current sources at the inputs. Transforming the equations of each mode, the following statements can be deduced:

For V_1-V_2 > $\frac{2 \cdot L \cdot F_{com} \cdot (I_1+I_2)^3}{I_1 I_2}$ then the converter has to work in CDCM or in CCM

For V_1-V_2 < $\frac{I_2 \cdot I_1}{C \cdot F_{com} \cdot (I_1+I_2)}$ then the converter has to work in VDCM or in CCM

Where F_{com} is the switching frequency, L the inductance, C the capacitance, and V_1,I_1,V_2 and I_2 the voltages and currents in each photovoltaic string respectively, as in previous chapters.

3.3 Design of the PV Strings

This project will focus on a 28KW photovoltaic system based on commercial Yingli Solar® YL300P-35b photovoltaic modules, and optimized for a commercial Ingeteam® INGECON SUN 3Play 28TL photovoltaic three-phase buck inverter. It consists of the following equipment:

Device	Quantity	Model	Nominal power
Photovoltaic modules	117	YL300-35b	300 Wp
Inverter	1	Ingecon Sun 3Play 28TL	28 kW

Table 3.1. Components of the photovoltaic systems.

Their main characteristics of them are exposed in the following tables 3.2 and 3.3:

Yingli YLP300P-35b Electrical parameters at Standard Test Conditions	
P_{max}	300 W
Voltage at P_{max}	35.8 V
Current at P_{max}	8.37 A
Open-circuit voltage V_{OC}	45.2 V
Short-circuit current I_{SC}	8.86 A
NOCT	46 ± 2 ºC
Temperature coefficient of V_{OC}	-0.32 %/ºC
Temperature coefficient of I_{SC}	0.05 %/ºC
Temperature coefficient of P_{max}	-0.42%/ºC
Electrical parameters at Nominal Operating Cell Temperature	
Voltage at P_{max}	32.7 V
Current at P_{max}	6.7 A
Open-circuit voltage V_{OC}	41.7 V
Short-circuit current I_{SC}	7.16 A

Table 3.2. Electrical parameters of the photovoltaic modules. [A.1]

INGECON SUN 3Play 28TL Electrical parameters	
Recommended PV power interval	28.9 kW – 37.5 kW
MPPT voltage interval	560 V – 820 V
Minimum DC voltage at the input	560 V
Maximum DC voltage at the input	1000 V
Maximum DC current	52 A
Maximum efficiency	98.5 %
Voltage at maximum efficiency	600 V

Table 3.3. Electrical parameters of the three-phase inverter. [A.2]

For further information, please check the attached official datasheets.

The worst conditions to analyse the system would be:

- 1000 W/m^2 of irradiance and 45ºC of ambient temperature for the voltage of the modules at P_{max} . Under these conditions, it has to be higher than the minimum DC voltage needed by the inverter → At least 19 series modules.

- 0 W/m^2 and -10ºC of ambient temperature for the voltage of the modules at V_{OC} . In these conditions, it has to be lower than the maximum DC voltage of the inverter → No more than 20 series modules.

These two scenes are sufficient to determine how many modules can be associated in series. Anyway, the same analysis will be carried out for the P_{max} voltages for those situations, in order to ensure there is no problem with it:

- For 1000 W/m^2 of irradiance and 45ºC of ambient temperature, the MPP voltage has to be higher than the minimum DC voltage needed by the inverter → At least 19 series modules.

- For 0 W/m^2 and -20ºC of ambient temperature, the MPP voltage has to be lower than the maximum DC voltage of the inverter → No more than 20 series modules.

The three-phase inverter allows small voltage variations in its DC bus. Therefore, only 19 and 20 series modules accomplish all the conditions, so that just three different configurations can be considered. In all of them, a symmetrical distribution of the modules to the strings requires an even number of parallel arrays.

- Three strings of 20 series modules in each input of the TIBuck converter. The mismatch losses would determine which strings goes in each input in order to accomplish that $V_{MPP,1}>V_{MPP,2}$.
- Three strings of 19 series modules in each input of the TIBuck converter. Again, the mismatch losses would determine which string goes in each input.
- 20 series modules can be situated in the first three strings, and 19 in the other three, so that for the same conditions $V_1>V_2$. This will be the chosen distribution for this application, although the other configurations result interesting too, as the MPP voltage of both strings would be very close, and so the voltage stress of the semiconductors.

  Furthermore, the P_{max} voltage of the strings in NOCT conditions is close to the maximum efficiency voltage of the inverter, which is always a good indicative.

3.4 Design of the Converter

Once the photovoltaic arrays have been designed, one has to focus on the converter. The converter has two different types of elements, which are treated separately in this chapter.

3.4.1 Semiconductors

At least 2 semiconductors are needed in this converter. For the proposed application, it can be assumed that $V_1>V_2$, so that only two are needed. One of them has to be an IGBT/MOSFET and the other can be a diode, as proved in chapter 3.1.

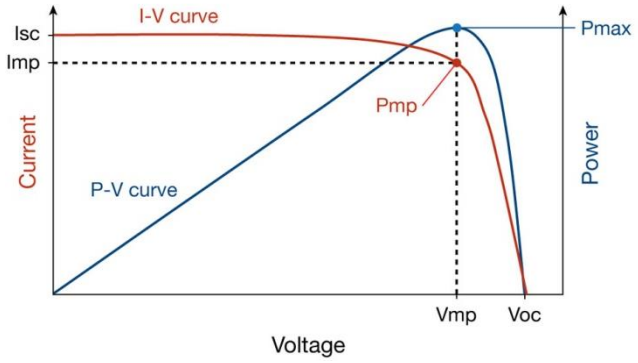

Figure 3.7. I-V and P-V curve of the photovoltaic cells [6].

Until the control is not designed, only the maximum current that might pass through the switch can be estimated as the sum of the short-circuit currents I_{sc} of the photovoltaic strings, which is close to the sum of the currents in the maximum power point of the strings I_{MP} , as observed in figure 3.7. Measurements in TONC conditions will be considered, as they are more realistic. That value results 2·21.48 = 42.96 A.

The next consideration that could be taken into account is that the working region of the system is the part of the I-V curve of the photovoltaic arrays between V_{MP} and V_{OC}. This assumption makes the maximum voltage V_1-V_2 which the switches suffer pretty small, around 215 V in the worst case (V_1=$V_{OC,1}$ and V_2=$V_{MPP,2}$) under TONC conditions, and would allow using MOSFET instead of IGBT as controlled switch, due to its higher commutation speed and its low losses.

Anyway, until the control of the converter is not designed, these conditions cannot be claimed because the maximum voltage difference V_1-V_2 may be altered by some other transitory effects, for example. Therefore the choice of the switches is postponed.

3.4.2 Passive elements

The passive elements include the inductor and the input capacitors. The output capacitor is the DC bus of the inverter, and as it is not the target of this project, it will not be analysed.

3.4.2.1 Input capacitors

In order to determine the value of the input capacitors, it is established that the MPPT losses caused by the voltage ripple at the input capacitors have to be lower than a 0.2%. [7] proves that these losses can be related with the voltage ripple of the capacitor of a photovoltaic array through the following expression:

$$\frac{P_{losses}}{P_{MP}} \approx \left(\frac{(\Delta V_C)_{rms}}{V_{MP}}\right)^2 \cdot \left(1+\frac{\frac{V_{MP}}{N}}{2 \cdot n \cdot V_T}\right) \quad (3.34)$$

Where P_{losses} are the power losses, P_{MP} is the maximum power, $(\Delta V_C)_{rms}$ is the rms value of the voltage ripple at the capacitor, V_{MP} is the voltage at the maximum power point, N is the number of cells considered, n is the diode characteristic parameter and V_T the thermal voltage.

Considering a Yingli YLP300P-35b photovoltaic module, which has 72 cells and the electrical parameters shown in table 3.2, the values needed to complete the expressions are:

V_{MP} in NOCT conditions = 32.7 V

N = 72 cells

And the parameters n and V_T are taken as the typical ones mentioned in the same article:

n = 1.4

V_T = 0.026 V

Introducing those values in the expression 3.34, one gets that:

$(\Delta V_C)_{rms}$ =0.543 V

As there will be only one input capacitor for 3 arrays of 19 photovoltaic series modules, then de real rms voltage ripple acceptable is 19 times higher, summing 10.33 V. The voltage ripple waveform can be approximated by a triangle wave, as shown in figure 3.38:

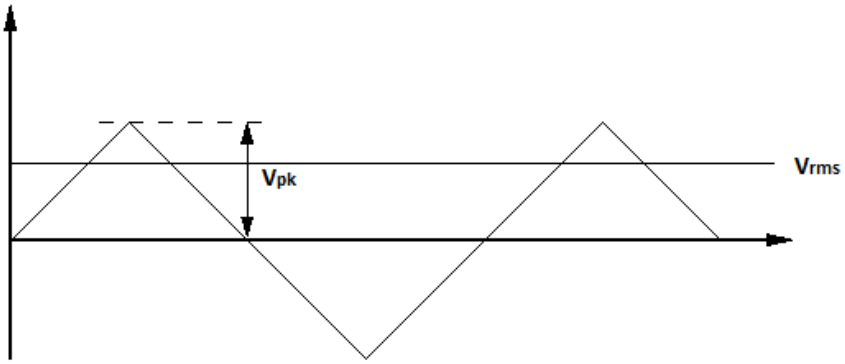

Figure 3.8. Triangular waveform.

It is well-known that the root mean square value of a triangle wave is related with its peak voltage with $V_{pk} = V_{rms} \cdot \sqrt{3}$ = 17.88 V. The voltage ripple ΔV_C is considered as $2 \cdot V_{pk}$ so the maximum voltage ripple tolerable for MPP losses below 0.2% results 35.77 V.

Once the maximum voltage ripple is determined, one has to size the capacitors. In any of the conduction modes, the expression that relates the voltage ripple with the capacitance is obtained from the fact that $<i_c>=0$, and is always the same:

$$\Delta V_C = \frac{I_1 \cdot (1-D)}{C \cdot F_{com}} \tag{3.35}$$

And solving it for the worst situation, one obtains that C_{min}=74.3 µF

Considering the worst situation with I_1 as the I_{SC} of the 3 parallel strings, and D=0. Then, from now on the capacitors will have a value of 75 µF.

3.4.2.2 The inductor

The inductor value will determine the current ripple at any time. In our system, the converter will work in CDCM only when the irradiance is very low, as the small voltage stress suffered by the inductor in normal conditions produces very small current ripple, making it very difficult for the converter to work in CDCM. In those situations the current ripple is lower than in CCM, so the CCM current ripple expression will be used to determine the inductance value:

$$\Delta i_L = \frac{(V_1 - V_2) \cdot D \cdot (1-D)}{L \cdot F_{com}} \tag{3.36}$$

If one derives the expression to obtain when does the maximum ripple take place, and solve it for L:

$$L = \frac{(V_{1,max} - V_{2,min})}{4 \cdot \Delta i_{L,max} \cdot F_{com}} \quad (3.37)$$

The maximum current ripple desired is taken as a 20% of the maximum inductor current i_L, which can reach $I_{SC1}+I_{SC2}$ = 53.2 A under STC conditions. That leads to a maximum admissible current ripple of 10.64 A.

As said before, if it can be guaranteed that the converter will always work between V_{MP} and V_{OC} in the I-V curve, then the maximum voltage stress under STC conditions would be:

$$V_{1,max}=V_{1,oc}=20 \cdot 45.2=904 \text{ V}$$
$$V_{2,min}=V_{2,MPP}=19 \cdot 35.8=680.2 \text{ V}$$

And subtracting them, one obtains that $V_{1,max}–V_{2,min}$=223.8 V. That leads to a required inductance of around 500 µH. However, STC conditions are not realistic for most of the applications, since it considers an irradiance of 1000 W/m^2 and 25ºC of module temperature. In order to have that module temperature, the needed ambient temperature can be deduced from the next equation:

$$T_c = \frac{G}{800} (NOCT-20)+T_a \quad (3.38)$$

Where T_c is the photovoltaic cell temperature, G is the irradiance, NOCT is the nominal operating cell temperature, and T_a is the ambient temperature. When using STC parameters (G=1000W/m^2, T_c=25ºC) and taking NOCT from the datasheet of the Yingli modules (46ºC) one gets that the ambient temperature needs to be -7.5ºC.

Therefore, for most of the locations an irradiance of 1000W/m^2 and an ambient temperature of -7.5ºC are exceptional conditions that may happen just a few times per year, or maybe never. Furthermore, it is very unlikely that one string operates in STC and the other in open circuit.

However, when working in other areas of the I-V curve, the voltage difference between the MPP of both strings could become greater than 223.8 V, when the strings have different irradiance or, less likely, when their operating temperatures are different.

Anyway, in order to be moderate, a 500 µH inductor will be considered and after designing the control of the converter, this value will be checked again.

3.5 Control of the Converter

In this converter there are two power inputs: one of them made up of 3 strings of 20 series modules, and the other of 3 strings of 19 series modules. In order to perform dual MPPT, it is clear that both input voltages have to be controlled.

The TIBuck makes use of two degrees of freedom: The duty cycle of the controlled switch (d) and the DC bus voltage of the inverter, V_{out} , which is the output voltage of the TIBuck. The duty cycle can be modified changing the modulated wave value during the pulse width modulation (PWM), and the output voltage can be adjusted with the voltage control loop performed by the inverter. Both degrees of freedom are needed to be controlled because both input voltages are wanted to be modified independently.

Figure 3.9. Control schematic.

Figure 3.9 represents the control block that is wanted to be designed. It calculates the value of the two degrees of freedom depending on the desired photovoltaic voltages at the input of the TIBuck converter.

Different strategies can be proposed to do this control. At first sight, controlling one of the input voltages with D and the other with V_{out} is the clearest option. However, along this project, it has been remarked how important is the value V_1-V_2, since it represents the voltage stress the semiconductors support. Furthermore, that value

represents the voltage stress supported by the inductor, and so it is directly related to the current ripple at it.

In conclusion, V_1-V_2 is a critical value that determines the design of the majority of elements of the converter, namely the semiconductors and the inductor. With all these facts, a very good choice would be to control the subtraction of the input voltages with one degree of freedom. Once V_1-V_2 is controlled, V_1 , V_2 , or another combination of them has be to controlled with the other degree of freedom in order to obtain the desired voltages at the inputs. From now on, V^+ will refer to $V_{1,ref}$ +$V_{2,ref}$, and V^- to $V_{1,ref}$ -$V_{2,ref}$, where $V_{1,ref}$ and $V_{2,ref}$ are the outputs of the MPPT algorithm.

As this project designs the TIBuck converter for a medium-power photovoltaic system of 30 kW, it will only be considered cascaded control loops with an inner current loop, as the extra level of robustness that it provides results essential for systems of this size.

Another thing that has to be considered is the rapidity of the output voltage control, which is performed by the inverter. As the this paper does not focus on the inverter, it will be considered a cut-off frequency of 60-70 Hz for that close-loop, which is a typical value in three-phase inverters as the one used for this application. Therefore, the external control loop which calculates $V_{out,ref}$ has to be slower in any case.

Finally, current and voltage sensors will be considered to work with a cut-off frequency of 1200 Hz, in order to filter the inductor current ripple at the switching frequency (10 kHz) well enough. This frequency will limit the maximum cut-off frequency of any control designed.

3.5.1 Control of V^+ with the duty cycle and V^- with the output voltage

With this option, the strategy is represented in figure 3.10. Two different control loops can be differentiated in it:

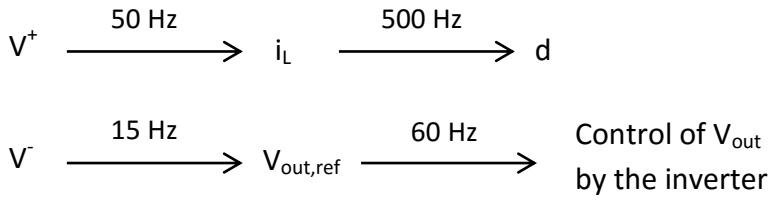

Figure 3.10. Schematic of the different control loops.

- V^+ is controlled through the duty cycle using a cascaded-loop. The inner loop controls the current at the inductor and, as it is a close loop, provides the security of controlling it at any moment, making the converter robust. It calculates the duty cycle needed to follow the inductor reference calculated by the external loop. Its cut-off frequency is set up at 500 Hz in order not to have problems with the measurements of the filter, whose cut-off frequency is 1200 Hz.

  The external loop works also as a close-loop, ensuring that V^+ follows its reference properly. As mentioned before, it calculates the reference for the inner current loop. Its cut-off frequency is situated a decade lower than the cut-off frequency of the inner current loop to ensure they are decoupled.

- V^- is controlled through the output voltage. The inner voltage close-loop is considered to be performed by the inverter at 60 Hz, so that the external loop has to be necessarily slower.

  The external control loop provides the reference for the inner loop performed by the inverter, and as it works in close-loop it ensures that V^- follows its reference. The low cut-off frequency of the inner loop restricts the rapidity of the external one. For this external loop, a cut-off frequency 4 times lower than the cut-off frequency of the inner loop is set up, in order to assume that both inner and outer loops are decoupled.

Firstly the cascaded-loop of V^+ will be designed, and afterwards the single control loop of V^-. The inner 60 Hz loop which controls V_{out} will not be designed, as it is performed by the inverter, and designing it is not the target of this project.

3.5.1.1 Inner control of the inductor current with the duty cycle

The equation that relates the current at the inductor and the duty cycle of the converter has to be obtained to analyse this loop. If one focus on the voltage at the inductor (see figure 3.1) one gets that:

$$v_L = L\frac{di_L}{dt} \tag{3.39}$$

$$v_1 \cdot d + v_2 \cdot (1-d) - v_{out} = L\frac{di_L}{dt} \tag{3.40}$$

And applying the Laplace transformation one obtains the expression that relates both the duty cycle and the inductor current:

$$I_L = \frac{D\cdot(V_1 - V_2) + V_2 - V_{out}}{L\cdot s} \tag{3.41}$$

With the transfer function of the system determined, the control can be designed using a proportional and integral (PI) controller with the appropriate compensations of the input and output voltages, as shown in the following scheme:

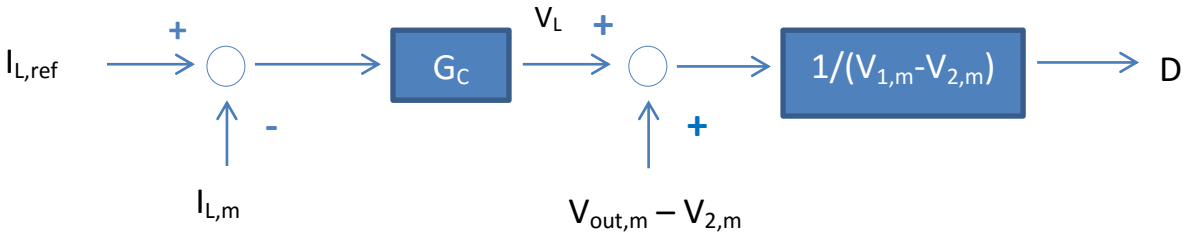

Figure 3.11. Scheme of the inner current loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference, and $I_{L,m}$, $V_{out,m}$, $V_{1,m}$ and $V_{2,m}$ the inductor current, the output voltage, and the input photovoltaic voltage measurements respectively.

The parameters of the loop are set up us shown in the next table:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	500 Hz
Phase margin	60º

Table 3.4. Parameters to design the controller #3.

Obtaining an optimal PI controller $G_C = \frac{1.687 \cdot (0.00246s+1)}{0.00246s}$

The close-loop transfer function of the system is represented in figure 3.12. The absolute magnitude of the response for a sine wave reference at the cut-off frequency of the loop is 1.08, while the expected delay between the reference and the response is 37.5 degrees.

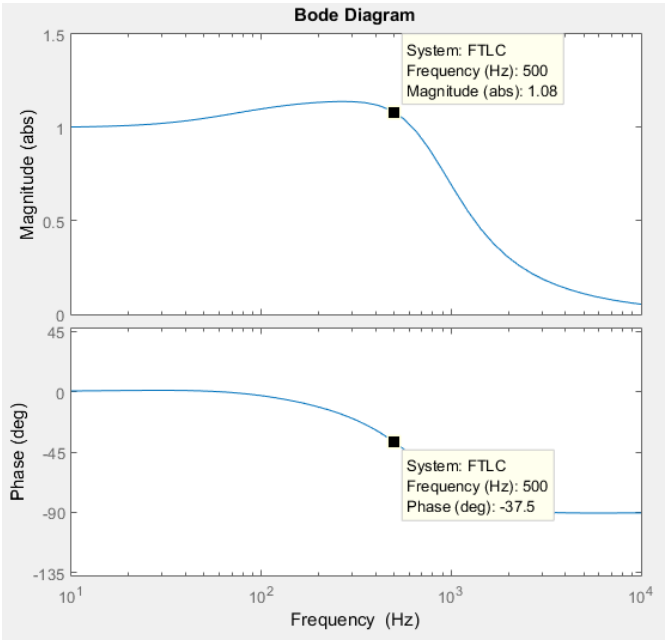

Figure 3.12. Close-loop transfer function of the system.

Theoretical results are verified by simulations, as shown in the next figures:

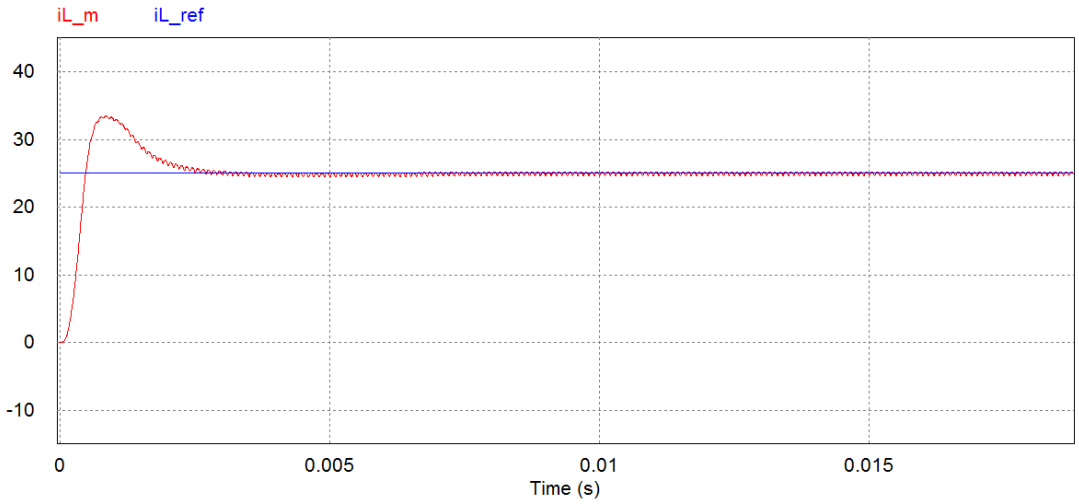

Figure 3.13. Response of the system for a DC reference.

Figure 3.13 shows that, for a DC reference, it achieves it quickly with an overshoot of around 18%.

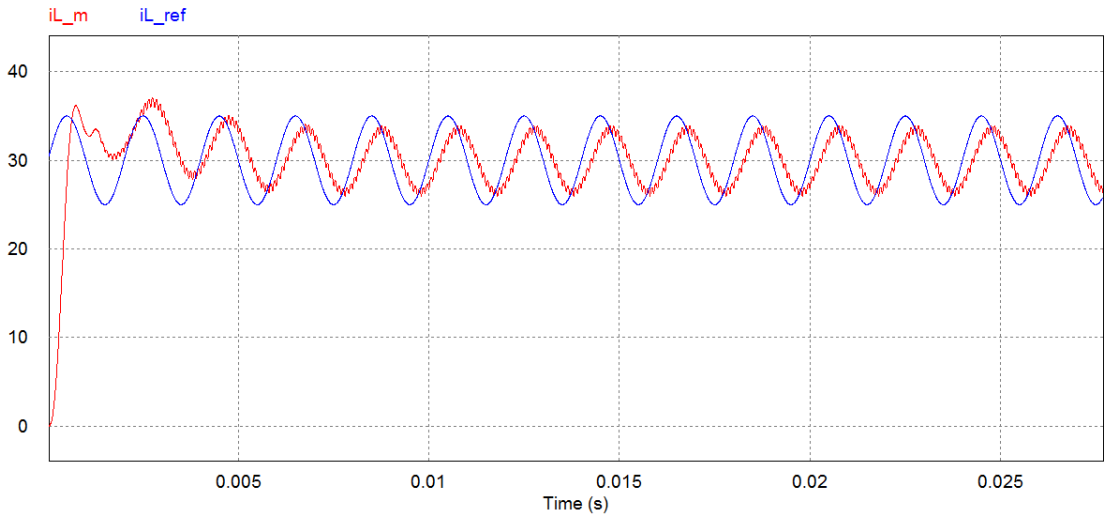

Figure 3.14. Response of the system for a 500 Hz sine wave reference.

Figure 3.14 shows that, for an AC sinusoidal reference at the cut-off frequency of the loop (500 Hz), it has smaller overshoot (<5%) and it achieves the reference rapidly as well. The delay of the measured inductor current (red wave) is around 60 degrees and the absolute magnitude around 0.7.

As this simulation compares the reference with the measured value, it needs to consider the effect of the filter at the cut-off frequency of the loop. In particular, the filter delays the measurement 22.62 degrees, and has an absolute magnitude of 0.923, so that the expected values for the measured response are around 22.6+37=59.6 degrees and an absolute magnitude of 1.06·0.923=0.98. Having said that, it can be noticed from figure 3.13 that the delay of the response results as expected, while the magnitude is considerably lower than awaited. However, for the moment this fact does not compromise the performance of the control.

With these verifications, the inner control loop is approved and now the external voltage loop has to be designed.

3.5.1.2 External control loop of V^+ with the inductor current

In this instance, the expression that relates V_1+V_2 with i_L has to be obtained. Analysing the equations at both input capacitors, one gets:

$$C\frac{dv_1}{dt} = i_1 - i_L \cdot d \quad (3.42)$$

$$C\frac{dv_2}{dt} = i_2 - i_L \cdot (1-d) \quad (3.43)$$

When summing them, and applying the Laplace transformation, the searched expression is found:

$$V^+ = V_1 + V_2 = \frac{I_1 + I_2 - I_L}{C \cdot s} \quad (3.44)$$

This expression is very illustrative. V^+ does not depend on the duty cycle, just on the inductor current I_L , so that controlling V^+ with the inductor current I_L makes sense.

Again the transfer function of the system has been determined, so that another control based on a proportional and integral controller with compensations can be designed as shown in figure 3.15:

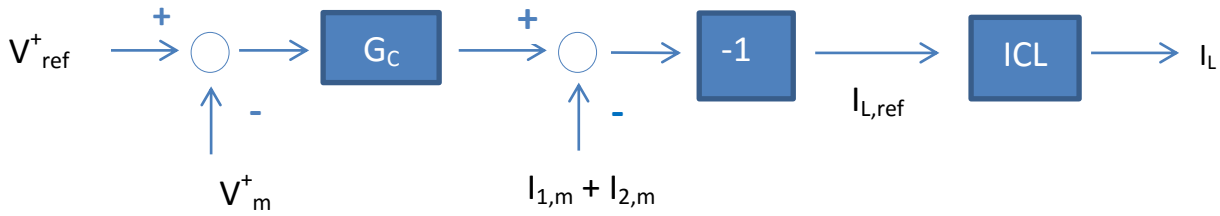

Figure 3.15. Scheme of the external voltage loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference, V^+_{ref} the sum of the desired voltages at the input photovoltaic arrays, and $V^+_{,m}$, $I_{1,m}$, $I_{2,m}$ the V^+ and the input photovoltaic current measurements respectively. ICL represents the inner current loop, which has been considered as a first order function with a pole at the cut-off frequency of the loop (500Hz).

The parameters of the loop are set up us follows:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	50 Hz
Phase margin	60º

Table 3.5. Parameters to design the controller #4.

Notice that the cut-off frequency of the loop has been set up a decade below the input loop's cut-off frequency to guarantee both are decoupled. The PI controller needed results $G_C = \frac{0.0237 \cdot (0.0792s+1)}{0.0792s}$

The close-loop transfer function of the system with the double control loop is represented in the following figure 3.16. It can be observed that the expected response of the system for a sine wave reference at the cut-off frequency of the loop is be 1.04 times bigger in amplitude, and delayed 53.8 degrees.

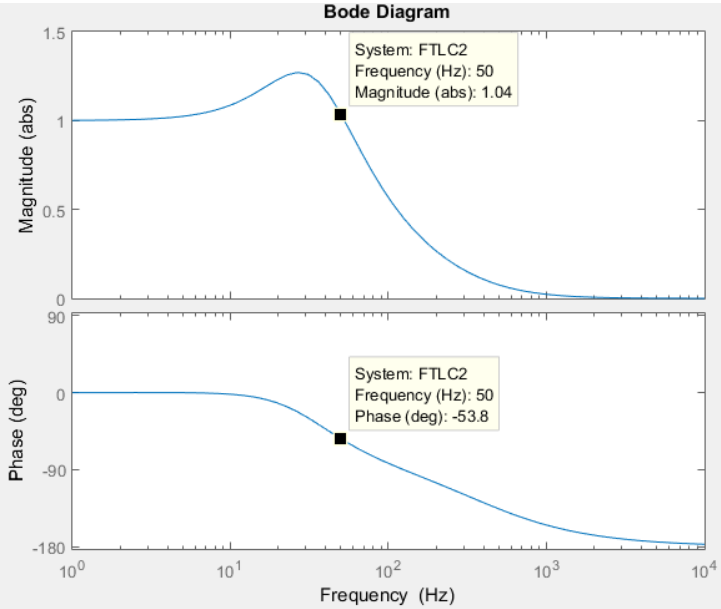

Figure 3.16. Close-loop transfer function of the system.

Now, the control is tested by simulations as shown in the following figures:

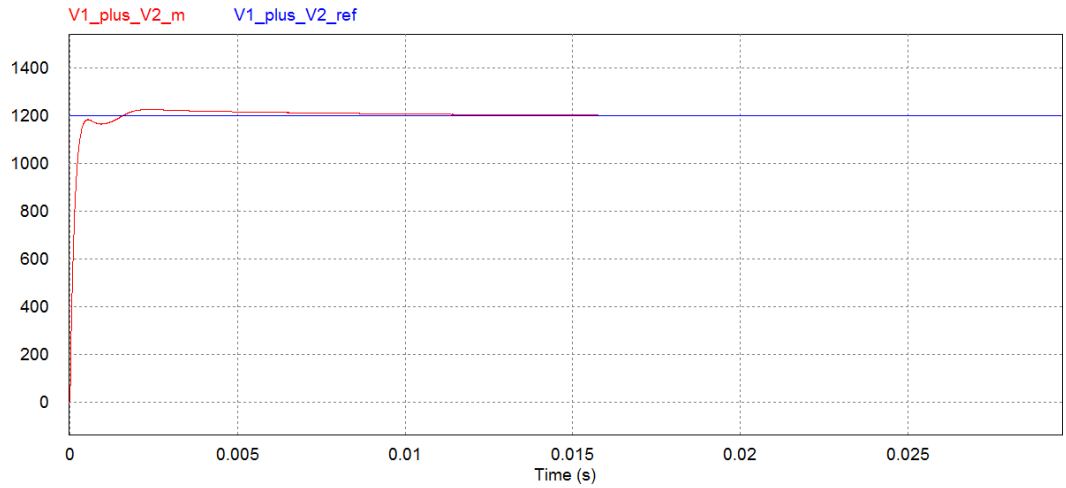

Figure 3.17. Response of the system for a DC reference.

In figure 3.17 can be observed that, for a DC reference, the system achieves it quickly and with very small overshoot.

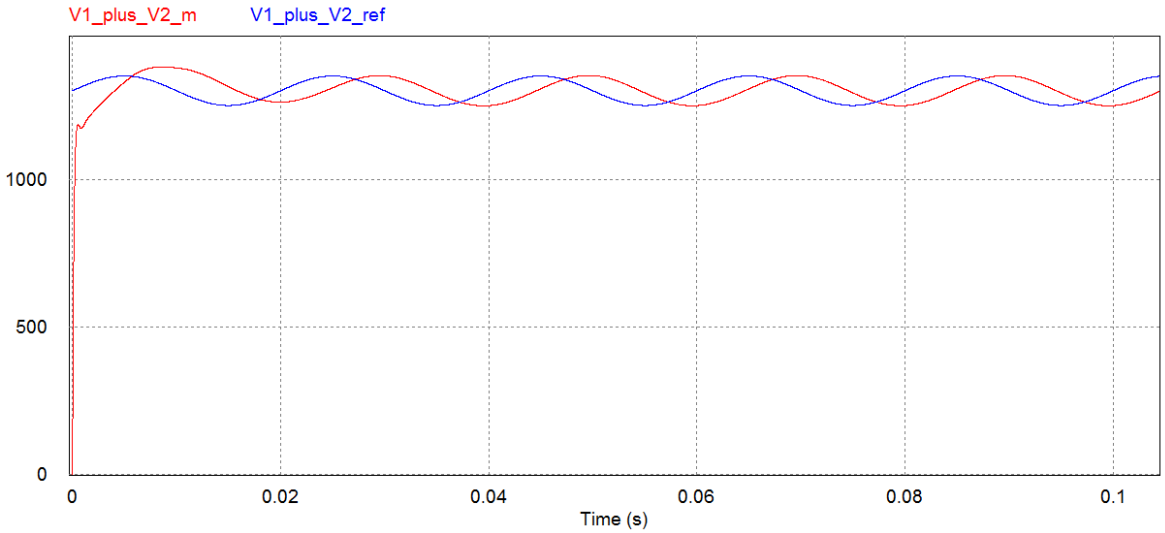

Figure 3.18. Response of the system for a 50 Hz sine wave reference.

Figure 3.18 shows the response of the system for a sine wave reference at the cut-off frequency of the loop. The results are similar that in the current loop: it achieves the reference quickly and with small overshoot, the delay between the reference (blue wave) and the measured current (red wave) is around 80 degrees, and the absolute magnitude slightly lower than 1.

The expected values for the delay and the absolute magnitude of the inductor current, considering the effect of the filter in the measurement at 50 Hz, were around 55 degrees and 1.04 respectively. The differences between the expectations and the behaviour observed in figure 3.18 affect mainly to the delay, and can be produced due to the approximation of the inner current loop as first order function, or because the compensations are not ideal. However, until the whole control system is designed, the effect of this factor cannot be properly judged.

At this point, two of the three loops have been designed and successfully verified. The sum V_1+V_2 is well controlled trough the duty cycle, and thus only V_1 , V_2 or a combination of them both has to be controlled with the output voltage to fully perform dual MPPT in CCM, which is the purpose of the project.

3.5.1.3 Control loop of the V¯with the output voltage

The same control philosophy is followed for this loop. The transfer function that relates V_{out} and V^- is needed to be determined in order to design the loop. If one analyses the expression of the voltage at the inductor (figure 3.1 can help), gets that:

$$v_L = L\frac{di_L}{dt} \tag{3.45}$$

$$v_1 \cdot d + v_2 \cdot (1-d) - v_{out} = L\frac{di_L}{dt} \tag{3.46}$$

Applying the Laplace transformation, the expression that relates both the output voltage V_{out} with V^- results:

$$V^- = \frac{V_{out} - V_2 + L\cdot s\cdot I_L}{D} = \frac{V_{out} - V_2 + V_L}{D} \tag{3.47}$$

Where V_L and D are calculated values from the first inner current loop control, which is very fast. In this expression, one can notice that nonlinearities appear and a simple control with compensations cannot be implemented.

With this scene, a small signal analysis is required in order to approximate those nonlinearities as a first order function, so that a suitable control without compensations that considers them can be designed. For this analysis, the real model of the photovoltaic module as a current source with a shunt resistance has to be considered, as represented in figure 3.19:

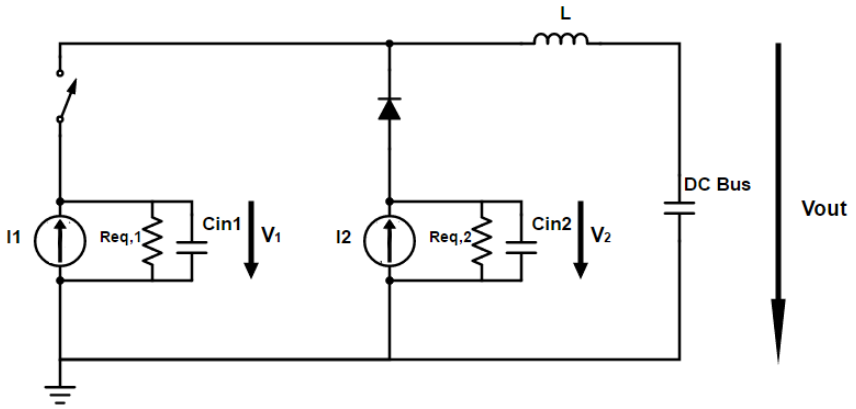

Figure 3.19. TIBuck converter using small-signal models of photovoltaic modules.

The shunt resistance of each input represent the point about which the I-V curve is linearized for the small-signal analysis, and its effect is treated more in depth in [11].

With this analysis, each variable can be divided into its DC value and its small-signal value. The following sign convention will be considered for the different parameters:

$$\overline{v_1} = V_1 + \widehat{v_1} \quad (3.48)$$

$$\overline{v_2} = V_1 + \widehat{v_2} \quad (3.49)$$

$$\overline{i_L} = I_L + \widehat{i_L} \quad (3.50)$$

$$d = D + \hat{d} \quad (3.51)$$

$$\overline{v_{out}} = V_{out} + \widehat{v_{out}} \quad (3.52)$$

Where the DC values are represented with capital letters, and the small-signal values are marked with a hat.

- Studying the equation of the current at the input capacitor 1 (3.5), one obtains:

$$\widehat{v_1} \cdot (Cs + \frac{1}{R_{eq,1}}) = -I_L \cdot \hat{d} - \widehat{i_L} \cdot D \quad (3.53)$$

- Analysing the equation of the current at the input capacitor 2 (3.6), one gets:

$$\widehat{v_2} \cdot (Cs + \frac{1}{R_{eq,2}}) = I_L \cdot \hat{d} + \widehat{i_L} \cdot (D-1) \quad (3.54)$$

- Studying the expression of the voltage at the inductor (3.4), one obtains:

$$\widehat{i_L} \cdot L \cdot s = \hat{d}(V_1 - V_2) + \widehat{v_2} \cdot (1-D) + \widehat{v_1} \cdot D - \widehat{v_{out}} \quad (3.55)$$

At this point, some considerations must be done:

- The inductor current i_L and V^+ are already controlled through the duty cycle. As the control loop of V^+ is several times faster than the control of V^- (due to the limitation of the inner voltage loop of V_{out}), it can be assumed that $V^+ = V^+_{ref}$, so that V^+ can be considered a disturbance when designing the control of V^- . As a result, $\widehat{v^-}$, the inductor current ($\widehat{i_L}$) , and the duty cycle ($\hat{d}$) can be expressed as functions of $\widehat{v^+}$ and the control variable, $\widehat{v_{out}}$.

- As a definition, $V^+ = V_1 + V_2$ and $V^- = V_1 - V_2$, so in the equations above $\overline{v_1}$ can be substituted with $\frac{\overline{v^+} + \overline{v^-}}{2}$ and $\overline{v_2}$ with $\frac{\overline{v^+} - \overline{v^-}}{2}$ where $\overline{v^+} = V^+ + \widehat{v^+}$ and $\overline{v^-} = V^- + \widehat{v^-}$.

With these two considerations, three new equations have to be set out:

$$\left.\begin{array}{l}\widehat{v^-}=f(\widehat{v^+},i_L,\hat{d})\\ \widehat{i_L}=f(\widehat{v^+},\hat{d},\widehat{v^-},\widehat{v_{out}})\\ \hat{d}=f(\widehat{v^+},i_L,\widehat{v^-})\end{array}\right\} \text{ And solve them obtaining } \left\{\begin{array}{l}\boxed{\widehat{v^-}=f(\widehat{v^+},\widehat{v_{out}})}\\ \widehat{i_L}=f(\widehat{v^+},\widehat{v_{out}})\\ \hat{d}=f(\widehat{v^+},\widehat{v_{out}})\end{array}\right.$$

The expression rounded in green is the one that interests for the control:

$$\widehat{v^-}=\widehat{v_{out}}\cdot\frac{2\cdot I_L}{\left[I_L\left(\frac{1}{R_{eq,1}}-\frac{1}{R_{eq,2}}\right)-V^-\cdot C\right]\cdot s+I_L\cdot(2D-1)+\frac{V^-}{R_{eq,1}}\cdot\left(D\cdot\left(1-\frac{R_{eq,1}}{R_{eq,2}}\right)-1\right)}+\widehat{v^+}\cdot FT_2 \qquad (3.56)$$

It is important to analyse expression 3.56 more in detail, because its complexity makes it impossible to draw conclusions with just having a look. It depends on different variable elements: I_L , $R_{eq,1}$, $R_{eq,2}$, V^- and D. The worst scene has to be considered to design the control, and the ranges of each parameter are shown in the next table:

Value	Minimum value	Maximum value
I_L	0 A	53.2 A
$R_{eq,1}$	3.091 Ω[11]	309.1 Ω[11]
$R_{eq,2}$	3.091 Ω[11]	309.1 Ω[11]
V^-	0 V	225 V*
D	0	1

Table 3.6. Limits for the variables of the transfer function.

***Considering that the photovoltaic arrays will only work between V_{MPP} and V_{OC} in the I-V curve.**

One way to approximate the worst situation would be to simulate how does the transfer function change with all the parameters. When analysing this, one gets that its phase change dramatically with the duty cycle as shown in figure 3.20:

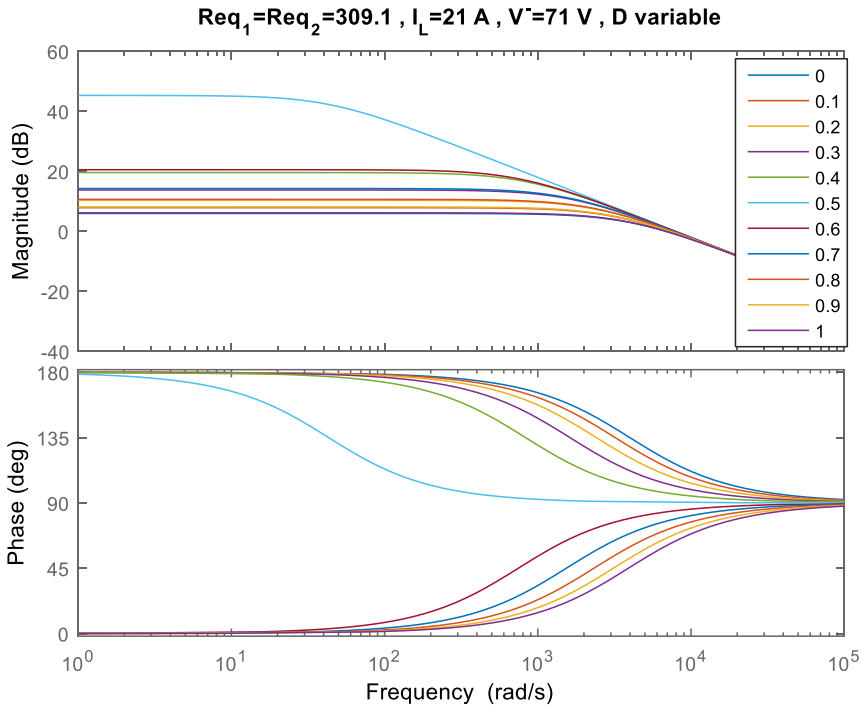

Figure 3.20. Bode diagram of the transfer function of the system depending on the duty cycle.

Figure 3.20 shows how does the term (2D-1) in the transfer function change the sign of the real part of the pole, and so changes the behaviour of the converter. It is clear to see that no controller can avoid that phase behaviour, and therefore this control cannot be implemented.

3.5.1.4 Control loop of V_1 with the output voltage

After analysing the system, it has been noticed that the suggested control of V^- is impossible to carry out. Thus, instead of controlling $V^-=V_1-V_2$ one could try to control one of the input voltages hoping that the effect of the term (2D-1) disappears. In this case, V_1 is wanted to be controlled using the remaining degree of freedom, V_{out}.

Again, it is needed to start with the same small-signal equations presented in chapter 3.5.1.3:

$$\widehat{v_1}\cdot\left(Cs+\frac{1}{R_{eq,1}}\right)= -I_L\cdot\hat{d} - \widehat{i_L}\cdot D \tag{3.57}$$

$$\widehat{v_2}\cdot\left(Cs+\frac{1}{R_{eq,2}}\right)= I_L\cdot\hat{d} + \widehat{i_L}\cdot(D-1) \tag{3.58}$$

$$\widehat{i_L}\cdot L\cdot s = \hat{d}(V_1-V_2)+ \widehat{v_2}\cdot(1-D)+ \widehat{v_1}\cdot D - \widehat{v_{out}} \tag{3.59}$$

In this case, the same considerations than in chapter 3.5.1.3 must be taken into account:

- The inductor current i_L and V^+ are already controlled through the duty cycle. As the control loop of V^+ is several times faster than the control of V_1 (due to the limitation of the inner voltage loop of V_{out}), it can be assumed that $V^+=V^+_{ref}$, so that V^+ can be considered a disturbance when designing the control of V_1 . As a result, $\widehat{v_1}$, the inductor current ($\widehat{i_L}$) , and the duty cycle ($\hat{d}$) can be expressed as functions of $\widehat{v^+}$ and the control variable, $\widehat{v_{out}}$.

- As a definition, $V_2=V^+-V_1$ so in the equations above $\overline{v_2}$ can be substituted with $\overline{v^+}-\overline{v_1}$ where $\overline{v^+} = V^+ + \widehat{v^+}$ and $\overline{v_1} = V_1 + \widehat{v_1}$

Now three new equations have to be set out:

$$\left.\begin{array}{l}\widehat{v_1}=f(\hat{d},\widehat{i_L})\\ \hat{d}=f(\widehat{v^+},i_L,\widehat{v_1})\\ \widehat{i_L}=f(\hat{d},\widehat{v_1},\widehat{v^+}\end{array}\right\} \quad \text{And solving them} \quad \left\{\begin{array}{l}\boxed{\widehat{v_1}=f(\widehat{v^+},\widehat{v_{out}})}\\ \hat{d}=f(\widehat{v^+},\widehat{v_{out}})\\ \widehat{i_L}=f(\widehat{v^+},\widehat{v_{out}})\end{array}\right.$$

The expression rounded in green is again the one that interests for the control:

$$\widehat{v_1}= \widehat{v_{out}}\cdot\frac{-I_L\cdot s}{\left[I_L\cdot L\cdot\left(\frac{1}{R_{eq,1}}-\frac{1}{R_{eq,2}}\right)+C\cdot(V_1-V_2)\right]\cdot s+I_L\cdot(1-2D)+\frac{(V_1-V_2)\cdot(1-D)}{R_{eq,1}}+\frac{D}{R_{eq,2}}(V_1-V_2)} + \widehat{v^+}\cdot FT_2 \qquad (3.60)$$

Once again the term (1-2D) appears, and makes the pole of the transfer function change the sign of its real part in a similar way that in the other attempt, as represented in figure 3.21.

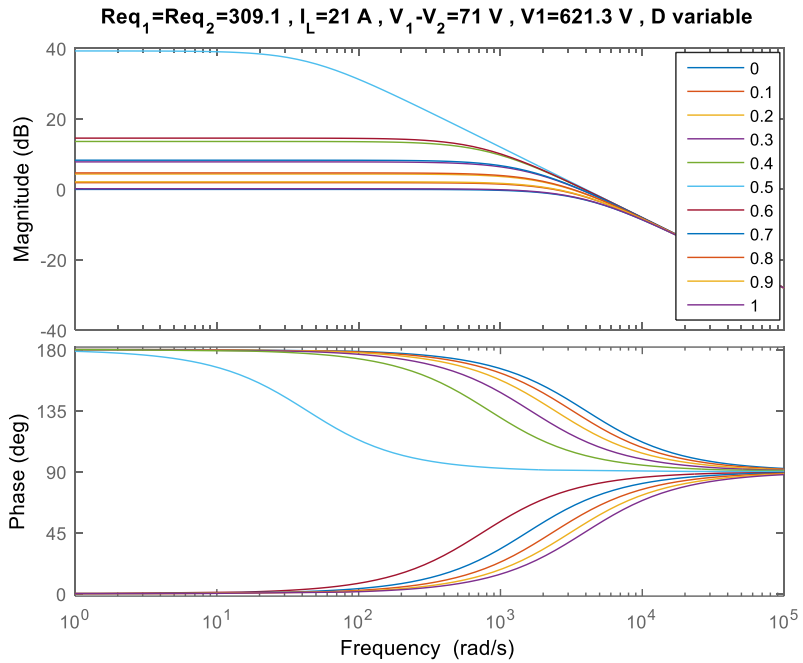

Figure 3.21. Bode diagram of the transfer function of the system depending on D.

Therefore, this control cannot be implemented and another strategy needs to be carried out to successfully control the photovoltaic voltages.

3.5.2 Control of V^+ with the output voltage and V^- with the duty cycle

As the last control strategy has not succeed, another strategy is proposed in figure 3.22:

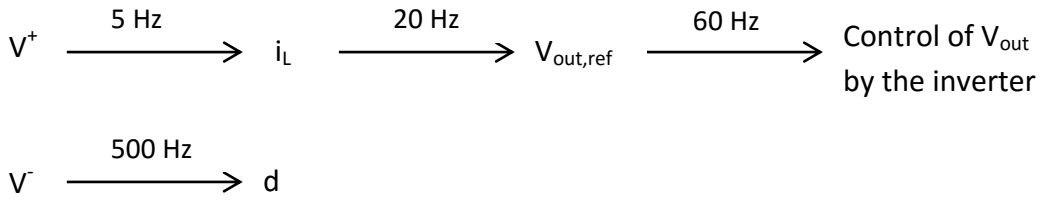

Figure 3.22. Schematic of the different control loops.

In this second attempt to perform dual MPPT in the converter, again two different control loops can be differentiated:

- In this case, V^+ is controlled with the output voltage instead of the duty cycle. This control is again carried out with a cascaded-loop since V^+ only depends on the inductor current (equation 3.44), what makes it very easy to relate both variables. The inner current close-loop provides robustness to the control, although in this case the control of V_{out} (performed by the inverter at 60 Hz) limits its rapidity. Nevertheless, situating the cut-off frequency of the loop at 20 Hz (3 times lower) allows controlling the inductor current quick enough, and decoupled from the control loop of V_{out}.

  On the other hand, the external voltage control loop of V^+ works also in close-loop, ensuring that V^+ follows its reference. However, its rapidity is also compromised by the inner current loop, making it hard to establish a cut-off frequency higher than 5 Hz, in order to ensure both loops work decoupled. Even so, 5 Hz is fast enough for this application.

- V^- is again controlled with the duty cycle using a single-loop structure, because the inner voltage loop performed by the inverter now must not be considered, as takes part in the other control loop. Thus, the limitation of the rapidity of the control disappears, and makes it possible to control V^- very fast, at 500 Hz. As mentioned in chapter 3.1, this parameter is very important since it represents the voltage stress of the semiconductors and the inductor, and is critical for designing the converter. Controlling it at 500 Hz guarantees that the maximum voltage supported by the semiconductors is never exceeded, providing even more robustness to the converter.

At first sight, the variables involved in each loop are related in an easier way than in the last strategy purposed, so the controlled is expected to succeed with fewer difficulties.

3.5.2.1 Control loop of V^- with the duty cycle

The first loop designed will be again the faster one, in this case the control loop of V^- through the duty cycle of the converter. The relation between V^- and D can be easily obtained analysing the current at both input inductors:

$$C\frac{dv_1}{dt} = i_1 - i_L \cdot d \tag{3.61}$$

$$C\frac{dv_2}{dt} = i_2 - i_L \cdot (1-d) \tag{3.62}$$

The desired transfer function of the system can be obtained subtracting them, and applying the Laplace transformation:

$$V^{-} = \frac{I_1 - I_2 + I_L \cdot (1-2D)}{C \cdot s} \tag{3.63}$$

A control based on a proportional and integral controller with easy compensations can be designed as shown in figure 3.23:

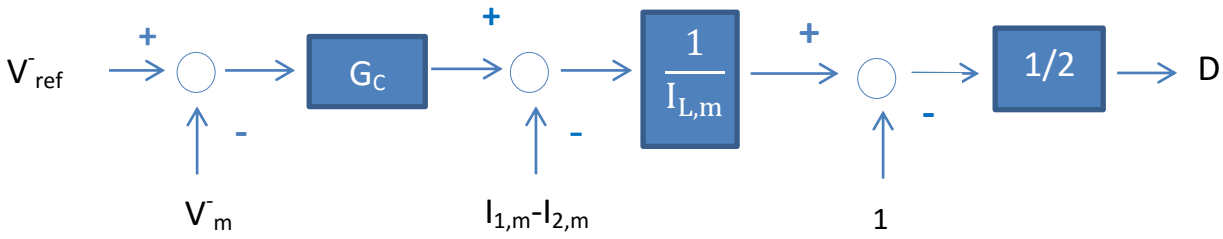

Figure 3.23. Scheme of the voltage loop.

Where G_C represents the PI controller, V^{-}_{ref} the V^{-} reference and $I_{1,m}$, $I_{2,m}$ and $i_{L,m}$ the photovoltaic and inductor current measurements respectively.

The parameters of the loop to design the controller are set up as represented in table 3.7:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	500 Hz
Phase margin	60º

Table 3.7. Parameters to design the controller #5.

And the suitable proportional and integral controller for this control loop is $G_C = \frac{0.2529 \cdot (0.00246s+1)}{0.00246s}$. The close-loop transfer function of the system with the controller and compensations is represented in figure 3.24. The expected absolute magnitude and the delay of the response for a sine wave reference at the cut-off frequency of the loop are 1.08 and 37.5 degrees respectively.

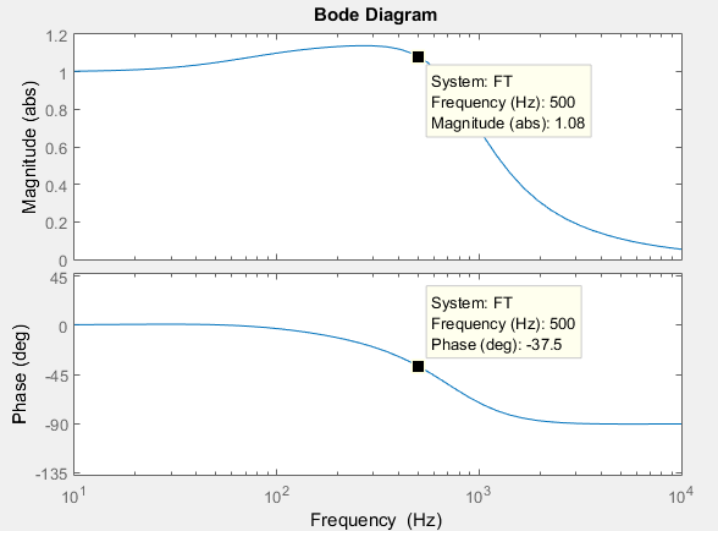

Figure 3.24. Close-loop transfer function of the system.

The theoretical behaviour of the system needs to be verified with different simulations as explained below.

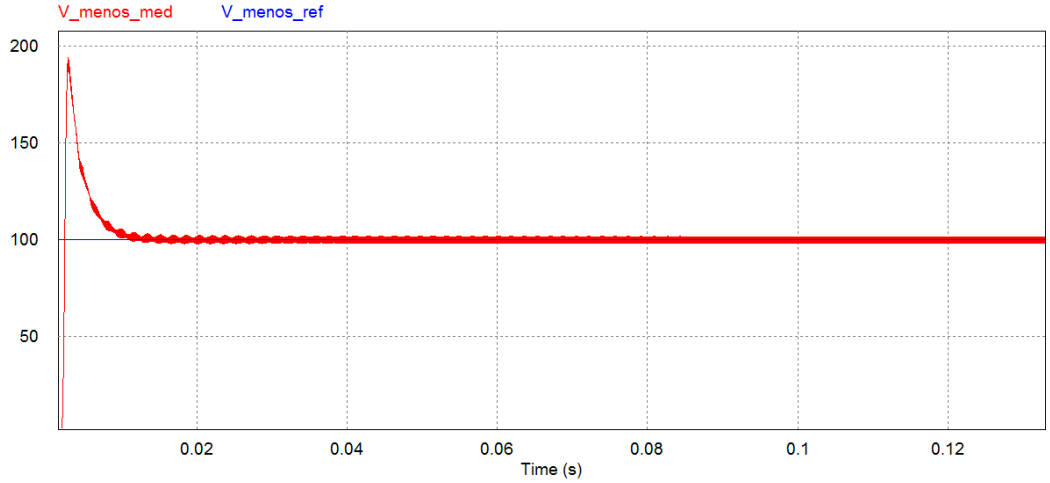

Figure 3.25. Response of the system for a DC reference.

Figure 3.25 shows that, for a DC reference, it achieves it very quickly but with an overshoot of almost 100%. The overshoot problem analysis will be postponed for the moment, until all the control loops are designed and verified, because parameters like the initial voltage of the input and output capacitors during the start-up influence significantly.

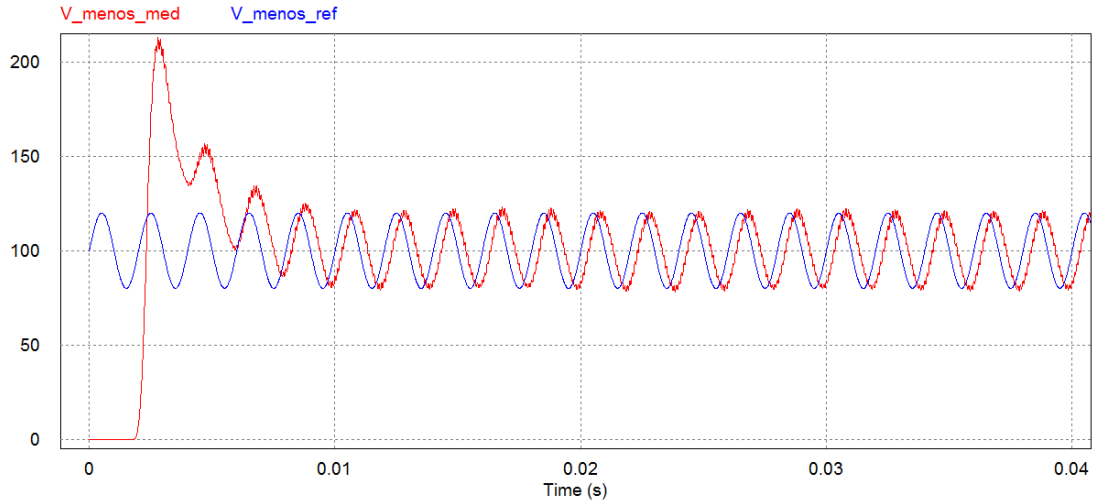

Figure 3.26. Response of the system for a 500 Hz sine wave reference.

In figure 3.26 can be observed that, for an AC reference, it achieves it quickly as well and the big overshoot observed before appears again. The delay between the reference and the response of the system is around 72 degrees, higher than the 60 degrees expected from the Bode diagram 3.22 and considering the delay added by the filter at 500 Hz. However, the magnitude of the response is around 1, as expected from the same diagram.

Therefore, this control loop is verified and the overshoot problem will be studied at the end of the control design as mentioned before.

3.5.2.2 Inner control loop of the inductor current with the output voltage

The inner loop that controls i_L with the output voltage is designed following the same techniques than in other occasions. Analysing the voltage at the inductor, one obtains:

$$v_1 \cdot d + v_2 \cdot (1 - d) - v_{out} = L \frac{di_L}{dt} \tag{3.64}$$

Applying the Laplace transformation, the expression results:

$$I_L = \frac{-V_{out} + D \cdot (V_1 - V_2) + V_2}{L \cdot s} \tag{3.65}$$

It can be observed that, compensating the duty cycle, and using a proportional and integral controller, the inductor current may successfully be controlled. The control loop is designed as represented in figure 3.27:

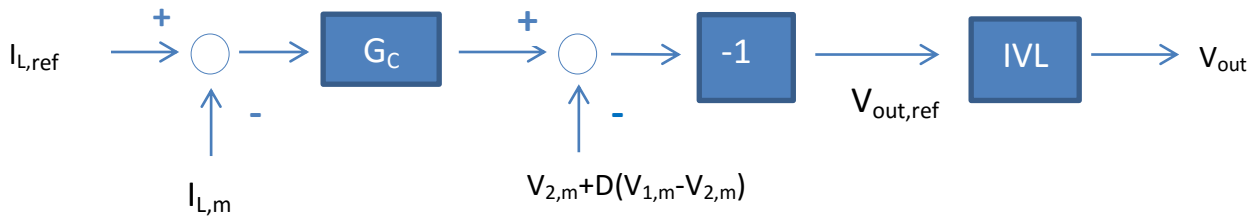

Figure 3.27. Scheme of the inner current loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference and $I_{L,m}$, $V_{1,m}$ and $V_{2,m}$ the inductor current and photovoltaic voltage measurements respectively. IVL represents the inner voltage loop performed by the inverter, which has been considered as a first order function with a pole at the cut-off frequency of the loop (60 Hz).

As compensations with D usually do not have good results due to its variability, it is preferred to substitute it with is steady-state value $D_{ss}=\frac{V_o-V_2}{V_1-V_2}$, changing the compensations as represented in the next figure:

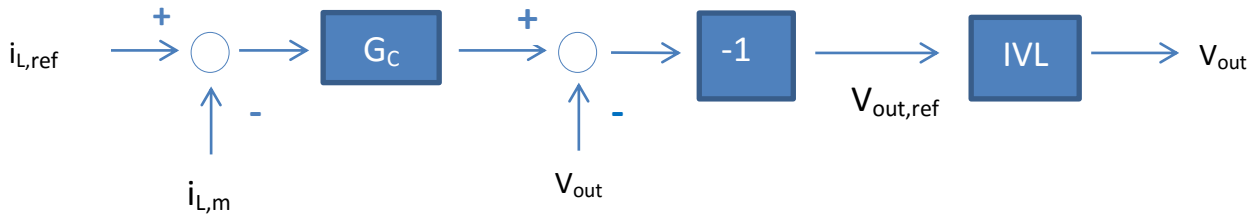

Figure 3.28. Scheme of the inner current loop using D_{ss} for the compensations

The parameters of the loop are set up us follows:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	20 Hz
Phase margin	60º

Table 3.8. Parameters to design the controller #6.

The ideal cut-off frequency of this loop would ideally be a decade below the cut-off frequency of the voltage loop performed by the inverter, but in that situation the external voltage loop that will be designed later would be too slow. Thus, a cut-off frequency 3 times lower than the voltage control loop of the inverter is set up. For those conditions, the PI controller needed results $G_C = \frac{0.0647 \cdot (0.042s+1)}{0.042s}$.

The close-loop transfer function of the system with the controller results as represented in figure 3.29. It shows that the expected absolute magnitude and the delay of the response for a sine wave reference at the cut-off frequency of the loop are 0.998 and 59.5 degrees respectively:

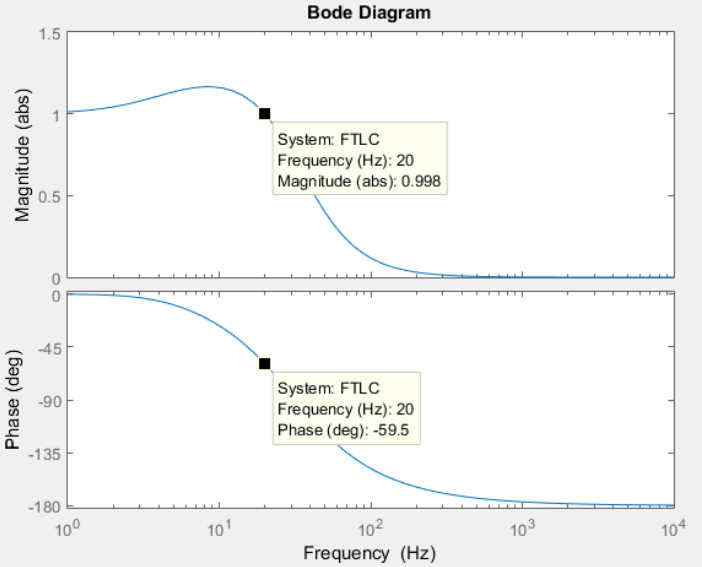

Figure 3.29. Close-loop transfer function of the system.

The theoretical behaviour of the system needs to be verified with simulations. For that, a fixed value for the duty cycle D has to be imposed during the simulations. One has to notice that, when simulating with the same I-V curve in both inputs of the converter, and working in continuous conduction mode, the steady state value of the duty cycle is $D = \frac{I_1}{I_1+I_2}$.

To accomplish that $V_1 > V_2$, one can deduce from the I-V curves represented in figure 3.30 that $I_2 > I_1$, and thus D has to be lower than 0.5.

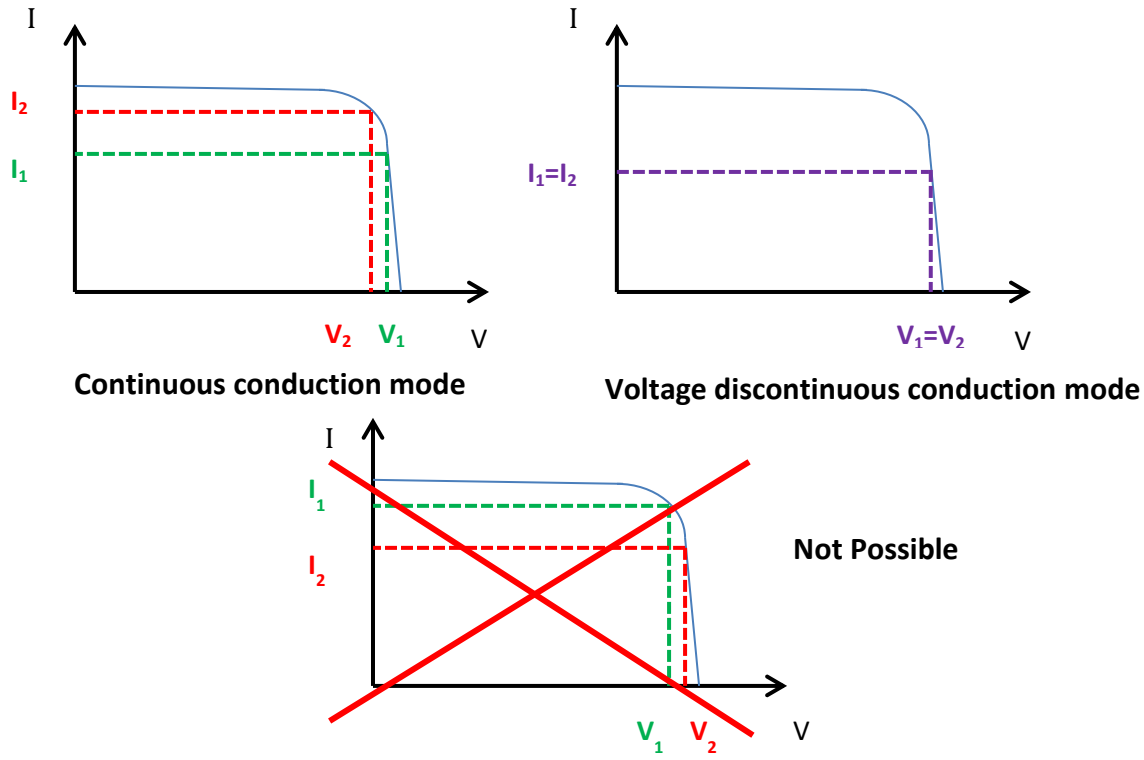

Figure 3.30. Explanation of why D has to be lower than 0.5 when testing the control.

In the limit situation where $I_1=I_2$ and D=0.5, $V_1=V_2$ and so the converter would work in voltage discontinuous conduction mode.

Having said that, the next simulations with a duty cycle of 0.3 will be carried out to validate the proposed current control loop:

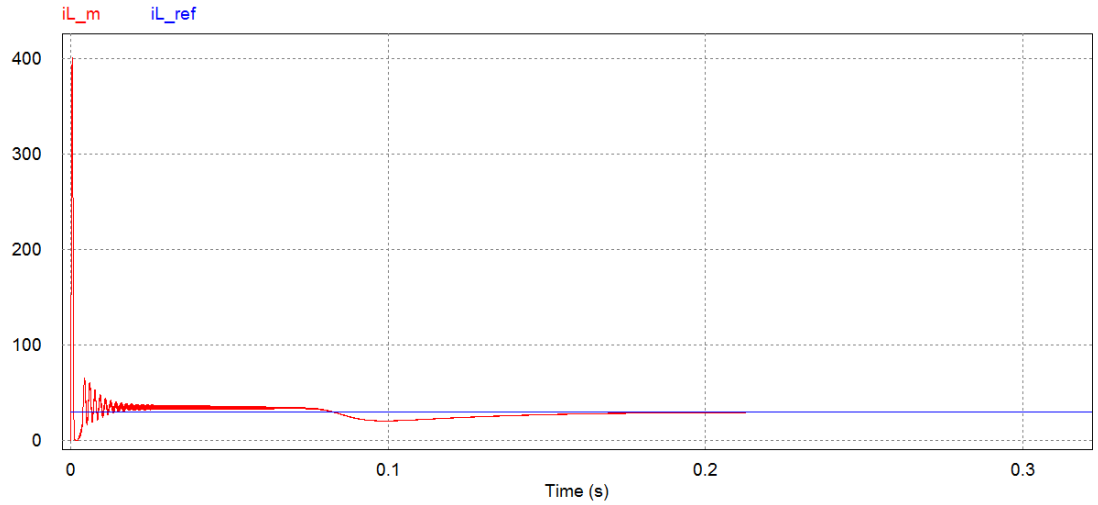

Figure 3.31. Response of the system for a DC reference using D_{ss} in the compensations.

Figure 3.31 shows that, for a DC reference, it needs around 0.3 seconds to achieve it, and has a disproportionate overshoot (400 A with a 30 A reference) at the beginning. In fact, the behaviour in the first 100 milliseconds is not as expected, probably to the effect of replacing D with its steady state value in the compensation. Considering the instant value of the duty cycle in the compensations, the behaviour changes as represented in figure 3.32:

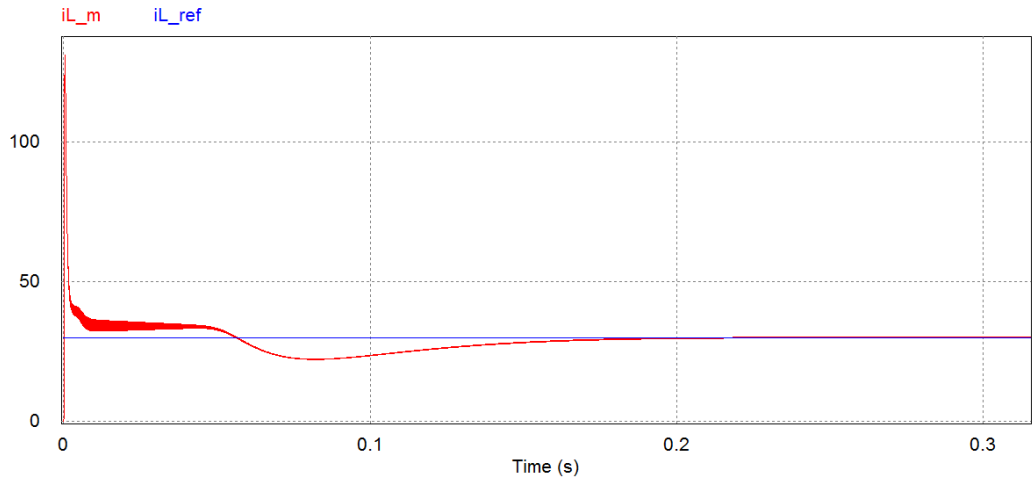

Figure 3.32. Response of the system for a DC reference compensating the instant value of D

It can be observed that the overshoot is reduced in 3 times, while still being disproportionate, and the settling time also reduces considerably.

The state-of-charge of the input capacitors at the beginning also modifies the overshoot of the response, but as in reality there will not be a situation with such a current reference step, this problem will not be treated until the whole control is designed and verified.

For an AC reference at the cut-off frequency of the loop, the performance of the system using the steady-state value of the duty cycle (D_{ss}) is represented in the next figure:

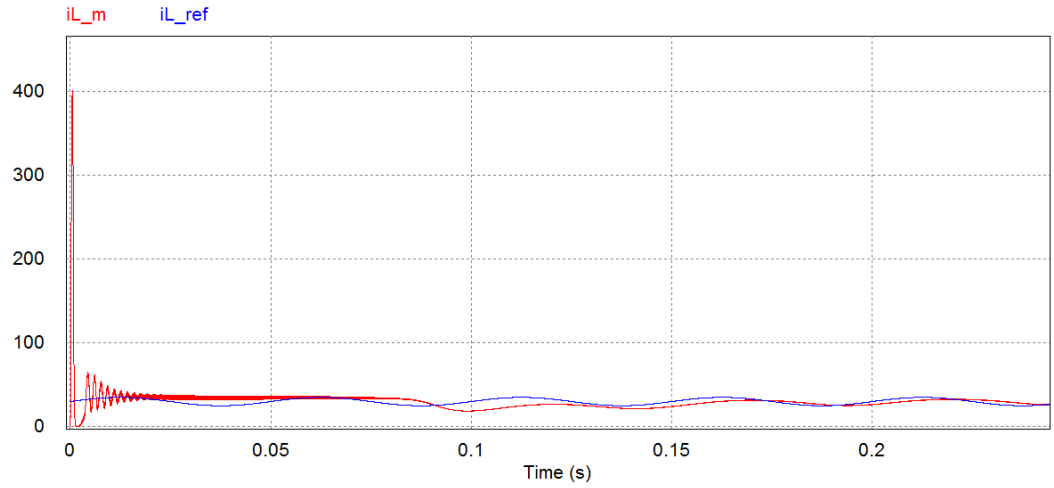

Figure 3.33. Response of the system for a 20 Hz sine wave reference compensating D_{ss}

Figure 3.33 shows that a tremendous overshoot appears again, and the settling time is similar to the case with a DC reference. The measured inductor current (red waveform) is delayed around 60 degrees as expected from figure 3.21, because the influence of the filter is very low at this frequency. However, the magnitude of the response is around 35% lower than expected from the same Bode diagram.

Considering the instant value of the duty cycle for the compensation, the behaviour is again better in every aspect, as shown in figure 3.34:

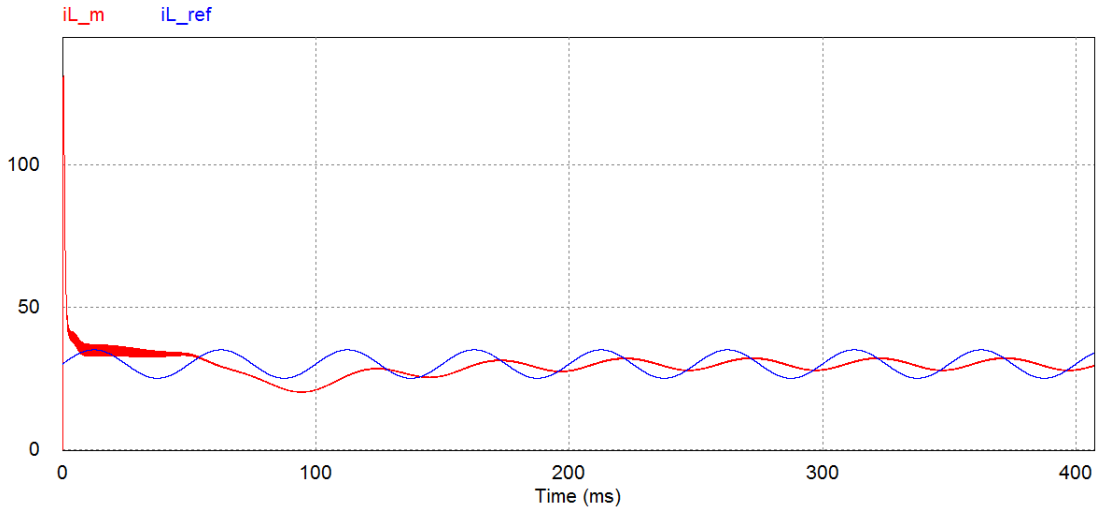

Figure 3.34. Response of the system for a 20 Hz sine wave reference compensating the instant value of D

The overshoot has been again reduced and the settling time is lower. Nevertheless, the delay of the measured variable is greater than before (72 degrees) and the magnitude around 55% lower than expected.

The differences between the expected behaviour and the reality are considerable, presumably due to the slow inner loop, which makes the compensations be very delayed, causing problems when working together with the external loop. Thus, a small-signal analysis could be the best option to design a control loop without compensations.

The starting point of the analysis are the same equations obtained in chapter 3.1 (Equations 3.4, 3.5 and 3.6).

$$\widehat{v_1}\cdot\left(Cs+\frac{1}{R_{eq,1}}\right)= -I_L\cdot\hat{d} - \widehat{i_L}\cdot D \tag{3.66}$$

$$\widehat{v_2}\cdot\left(Cs+\frac{1}{R_{eq,2}}\right)= I_L\cdot\hat{d} + \widehat{i_L}\cdot(D-1) \tag{3.67}$$

$$\widehat{i_L}\cdot L\cdot s = \hat{d}(V_1-V_2)+ \widehat{v_2}\cdot(1-D)+ \widehat{v_1}\cdot D - \widehat{v_{out}} \tag{3.68}$$

However, it has to be taken into account again that $\overline{v_1}$ can be substituted with $\frac{\overline{v^+}+\overline{v^-}}{2}$ and $\overline{v_2}$ with $\frac{\overline{v^+}-\overline{v^-}}{2}$ where $\overline{v^+} = V^+ + \widehat{v^+}$ and $\overline{v^-} = V^- + \widehat{v^-}$. The control loop of V^- is very fast, so that it can be assumed that $V^-=V^-_{ref}$, and V^- becomes a disturbance for the current control. Thus, $\widehat{v^+}$, $\widehat{i_L}$ and $\hat{d}$ can be expressed in terms of $\widehat{v^-}$ and $\widehat{v_{out}}$.

$$\left.\begin{array}{l}\widehat{v^+} = f(\hat{d}, \widehat{i_L}, \widehat{v^-})\\ \hat{d} = f(\widehat{v^+}, i_L, \widehat{v^-})\\ \widehat{i_L} = f(\hat{d}, \widehat{v^-}, \widehat{v^+}, \widehat{v_{out}})\end{array}\right\} \text{ And solving them } \left\{\begin{array}{l}\widehat{v^+} = f(\widehat{v^-}, \widehat{v_{out}})\\ \hat{d} = f(\widehat{v^-}, \widehat{v_{out}})\\ \boxed{\widehat{i_L} = f(\widehat{v^-}, \widehat{v_{out}})}\end{array}\right.$$

The expression rounded in green is the one that interest for the control:

$\widehat{i_L}=$

$\widehat{v_{out}}\cdot$

$$\frac{-2\cdot I_L C^2\cdot s - I_L\cdot C\cdot\left(\frac{3}{R_{eq,1}}+\frac{1}{R_{eq,2}}\right) - I_L\cdot\left(\frac{1}{R_{eq,1}^2}+\frac{1}{R_{eq,1}\cdot R_{eq,2}}\right)}{2\cdot I_L\cdot L\cdot C^2\cdot s^3 + C\cdot\left[I_L\cdot L\cdot\left(\frac{3}{R_{eq,1}}+\frac{1}{R_{eq,2}}\right)+C\cdot(V_1-V_2)\cdot(2D-1)\right]\cdot s^2 + \left[I_L\cdot\left(\frac{L}{R_{eq,1}}\cdot\left(\frac{1}{R_{eq,1}}+\frac{1}{R_{eq,2}}\right)+C\right)\right.}$$
$$\left. + \frac{C}{R_{eq,1}}\cdot(V_1-V_2)\cdot(3D-2)\right]s + \frac{(V_1-V_2)}{R_{eq,1}}\cdot\left(\frac{D-1}{R_{eq,1}}+\frac{D}{R_{eq,2}}\right)+\frac{I_L}{R_{eq,1}}$$

$+ \widehat{v^-}\cdot FT_2$ (3.69)

This complex expression again needs to be deeply analysed to see how does it change with the different parameters.

However, the first parameter analysed will be the duty cycle since it produced many problems in the previous chapter, and as the term (2D-1) appears again in the poles. This analysis is represented in figure 3.35:

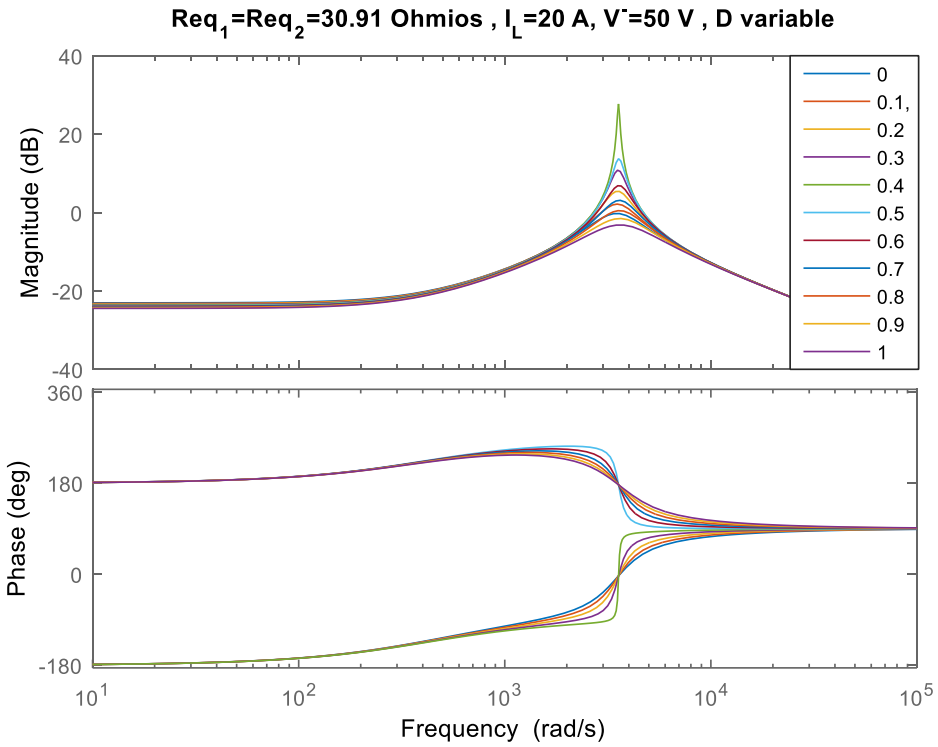

Figure 3.35. Bode diagram of the system depending on the duty cycle.

It shows that, for typical values of the parameters involved in the equation, the term (2D-1) of the poles again change their real parts, making the system uncontrollable as observed in the phase graph of the Bode diagram. Therefore, this strategy cannot succeed either and another one has to be thought.

3.5.2.3 Conclusions about controlling V^-

Other control strategies have been analysed, and in all of them the term (2D-1) appeared in the poles, changing the sign of their real parts depending on the operation point of the converter. Therefore no control of V^- can be carried out, as in any of them as soon as V^+ or V^- has successfully been controlled, the other variable cannot be controlled due to the term (2D-1). This fact is expected not to occur when controlling each photovoltaic voltage with one degree of freedom, so similar control strategies are wanted to be implemented with this new methodology. In order to avoid the problem of controlling V^-, another solution will be proposed in the next chapters.

3.5.3 Control of V_1 with the duty cycle and V_2 with the output voltage

This option comes from chapter 3.5.1, by replacing V^+ and V^- with the input voltages V_1 and V_2, as shown in the next schematic:

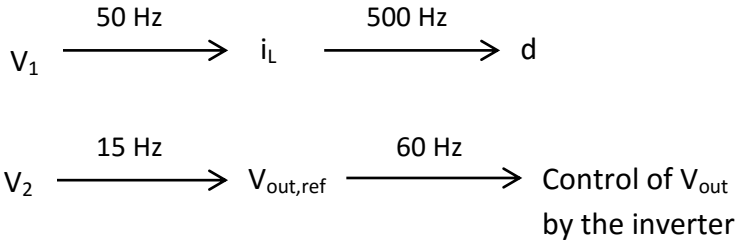

Figure 3.36. Schematic of the different control loops.

Figure 3.36 represents the control strategy for this attempt. Similarities clearly can be observed when comparing it with figure 3.10. Again, two different control loops can be differentiated:

- V_1 is controlled through the duty cycle using a cascaded-loop. The inner loop controls the current at the inductor and, as it is a close loop, provides more reliability. It calculates the duty cycle needed at any moment to follow the inductor reference calculated by the external loop. Its cut-off frequency is set up at 500 Hz in order not have problems with the measurements of the filter, whose cut-off frequency is 1200 Hz.

  The external loop works also as a close-loop, ensuring that V_1 follows its reference properly. As mentioned before, it calculates the reference for the inner current loop. Its cut-off frequency is situated a decade lower than the cut-off frequency of the inner current loop to ensure they are decoupled.

- V_2 is controlled through the output voltage. The inner voltage loop is considered to be performed by the inverter at 60 Hz, so that only the external loop needs to be designed. However, it has to be taken into account that the external loop has to be slower than the inner one.

The external control loop provides the reference for the inner loop performed by the inverter, and it works in close-loop. The low cut-off frequency of the inner loop restricts the rapidity of the external one. For this external loop, a cut-off frequency 4 times lower than the 60 Hz of the inner loop is set up, in order to assume that both inner and outer loops are decoupled. Its dynamic will be slower than the control loop of V_1.

Firstly the cascaded control loop of V_1 will be designed, and then the simple control loop of V_2, since the inner 60 Hz loop is performed by the inverter as explained before.

3.5.3.1 Inner control loop of the inductor current with the duty cycle

This loop has already been designed and verified for the same conditions in 3.5.1.1, so it will only be represented in figure 3.37 as a reminder:

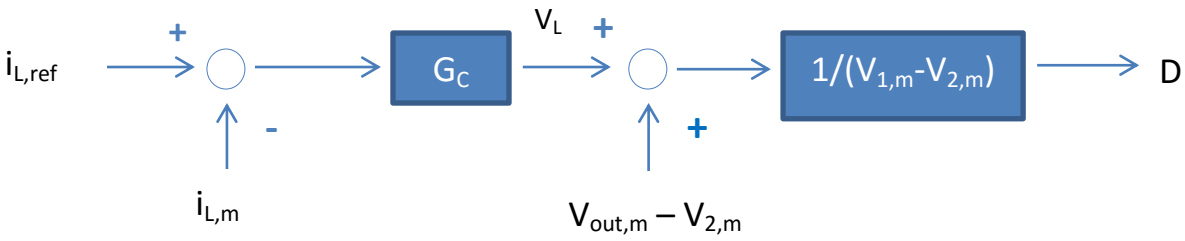

Figure 3.37. Scheme of the inner current loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference, and $i_{L,m}$, $V_{out,m}$, $V_{1,m}$ and $V_{2,m}$ the inductor current, the output voltage, and the input photovoltaic voltages measurements respectively. The optimal proportional and integral controller needed is $G_C = \frac{1.687 \cdot (0.00246s+1)}{0.00246s}$

3.5.3.2 External control loop of V_1 with the inductor current

This external loop does not change significantly from the one considered in 3.5.1.2. In this case, only the expression of the current at the capacitor 1 is needed:

$$C\frac{dv_1}{dt} = i_1 - i_L \cdot d \qquad (3.70)$$

Applying the Laplace transformation, it is easy to obtain the transfer function of the system:

$$V_1 = \frac{I_1 - I_L \cdot D}{C \cdot s} \tag{3.71}$$

It can be observed that, when compensating the duty cycle (D), the plant system can be controlled. The control scheme based on another PI controller and compensations is represented in figure 3.38:

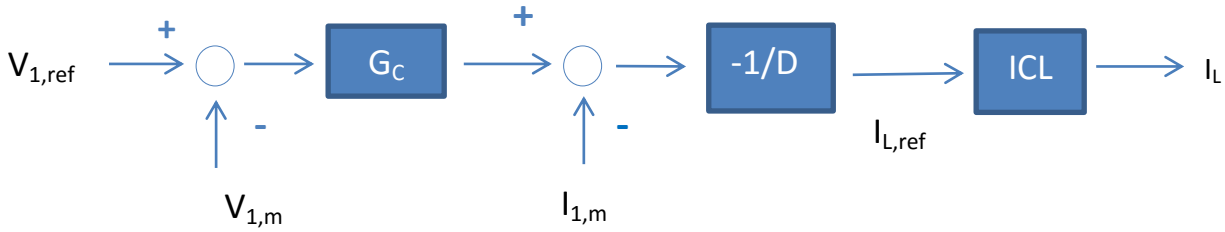

Figure 3.38. Scheme of the external voltage loop.

Where G_C represents the PI controller, $I_{L,ref}$ the inductor current reference and $I_{1,m}$ and $V_{1,m}$ the photovoltaic current and voltage measurements respectively. ICL represents the inner current loop designed in last section (3.5.3.2).

The following parameters are set up in order to determine the controller needed:

Commutation frequency	10000 Hz
Measurement filters' cut-off frequency	1200 Hz
Loop cut-off frequency	50 Hz
Phase margin	60º

Table 3.9. Parameters to design the controller #7.

With them, the optimal PI controller results $G_C = \frac{0.022 \cdot (0.0079s+1)}{0.0079s}$. The full system close-loop plant is represented in figure 3.39. At the cut-off frequency of the system, it has an absolute magnitude of 1 and a delay of 57.6 degrees when following a sine wave reference.

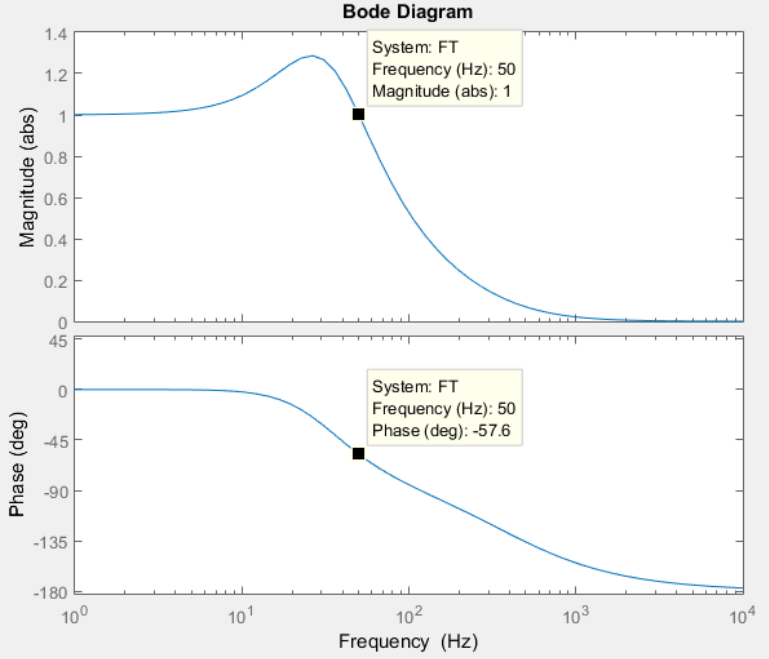

Figure 3.39. Bode diagram of the close-loop transfer function of the system.

Observing it, the expected response of the system for a sine wave reference would be another sine wave of the same magnitude but delayed 57.6 degrees. Different simulations must verify this behaviour, with a constant voltage source at the output of a lower value than the input voltage reference, as follows:

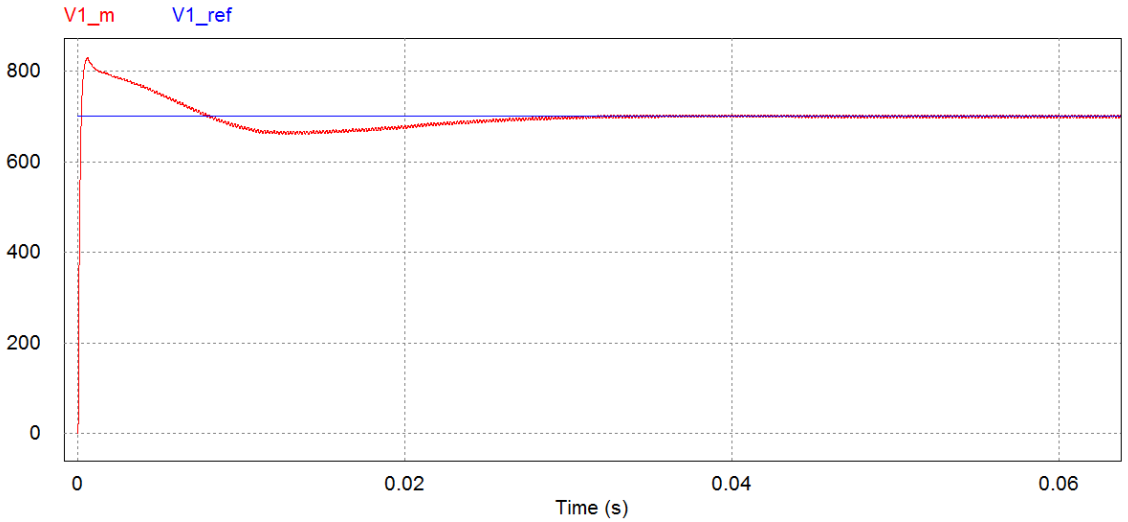

Figure 3.40. Response of the system for a DC reference.

Figure 3.40 shows that, for a DC reference, it achieves it quickly and with an overshoot of around 19 %.

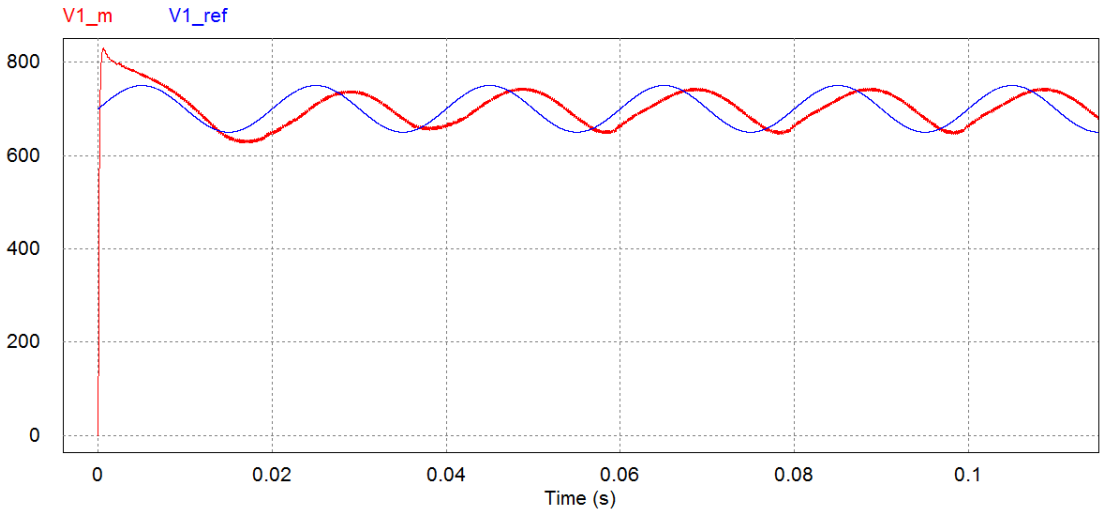

Figure 3.41. Response of the system for a 50 Hz sine wave reference.

Figure 3.41 tests the response of the system for a sine wave reference, showing that the system achieves it quickly as well, with a similar overshoot that in figure 3.37. The magnitude of the response is around 1 as expected, and its delay about 65º. Considering the delay introduced at 50 Hz by the filter, the expected value would be 60 degrees, so the delay is slightly higher than predicted. In addition, the response of the system is not a perfect sine wave. Anyway, this fact is not alarming and does not alter the correct operation of the system.

Now that the double control loop has been verified, the second photovoltaic array voltage is the only thing that still needs to be controlled to perform dual MPPT.

3.5.3.3 Control loop of V_2 with the output voltage

Designing this control loop requires analysing the voltage at the inductor expression and applying the Laplace transformation like in previous occasions:

$$L \cdot s \cdot I_L = V_1 \cdot D + V_2 \cdot (1-D) - V_{out} \quad (3.72)$$

The situation is analogous to the one analysed in chapter 3.5.1.3. Nonlinearities appear, so that a simple control with compensations cannot be carried out. Thus, a small signal analysis is needed in order to make it possible to implement a control loop without compensations.

The starting point of the analysis are the same equations obtained chapter 3.5.1.3, but the final expressions change:

$$\widehat{v_1} \cdot (Cs + \frac{1}{R_{eq,1}}) = -I_L \cdot \hat{d} - \widehat{i_L} \cdot D \quad (3.73)$$

$$\widehat{v_2} \cdot (Cs + \frac{1}{R_{eq,2}}) = I_L \cdot \hat{d} + \widehat{i_L} \cdot (D-1) \quad (3.74)$$

$$\widehat{i_L} \cdot L \cdot s = \hat{d}(V_1 - V_2) + \widehat{v_2} \cdot (1-D) + \widehat{v_1} \cdot D - \widehat{v_{out}} \quad (3.75)$$

In this case, similar but not exactly the same considerations must be taken into account when doing the small-signal analysis:

The inductor current i_L and V_1 are already controlled through the duty cycle. As the control loop of V_1 is several times faster than the control of V_2 (due to the limitation of the inner voltage loop of V_{out}), it can be assumed that $V_1=V_{1,ref}$, so that V_1 can be considered a disturbance when designing the control of V_2 . As a result, $\widehat{v_2}$, the inductor current ($\widehat{i_L}$) , and the duty cycle ($\hat{d}$) can be expressed as functions of $\widehat{v_1}$ and the control variable, $\widehat{v_{out}}$.

$$\left.\begin{array}{l} \hat{d} = f(\widehat{i_L}, \widehat{v_1}) \\ \widehat{v_2} = f(\widehat{i_L}, \hat{d}) \\ \widehat{i_L} = f(\hat{d}, \widehat{v_1}, \widehat{v_2}, \widehat{v_{out}}) \end{array}\right\} \text{ And solving them } \left\{\begin{array}{l} \hat{d} = f(\widehat{v_1}, \widehat{v_{out}}) \\ \widehat{v_2} = f(\widehat{v_1}, \widehat{v_{out}}) \\ \widehat{i_L} = f(\widehat{v_1}, \widehat{v_{out}}) \end{array}\right.$$

The expression rounded in green is the one that interest for the control:

$$\widehat{v_2} = \widehat{v_{out}} \cdot \frac{I_L}{I_L \cdot L \cdot C \cdot s^2 + \left[C \cdot D \cdot (V_1 - V_2) + \frac{I_L \cdot L}{R_{eq,2}}\right] + I_L \cdot (1-D) + \frac{D \cdot (V_1 - V_2)}{R_{eq,2}}} + \widehat{v_1} \cdot FT_2 \quad (3.76)$$

The term (2D-1) that made the plant uncontrollable now does not appear and the poles do not change their real part, which is a good indicative. In the expression, 4 terms are involved, and change it depending on their values.

When a deeper analysis is carried out, it is found that the most restrictive plant in terms of phase and cut-off frequency occurs when the following facts take place at the same time:

- The duty cycle D is maximum.
- The inductor current I_L in minimum.
- The equivalent shunt resistance of the second photovoltaic string small signal model is maximum.
- The difference between the voltages in both photovoltaic strings is minimum.

All of them cannot happen at the same time; for example, when the equivalent shunt resistance of the second photovoltaic string small signal model is maximum, the current is close to I_{SC}.

If all the conditions together are too restrictive the real worst plant of the system will need to be determined, though first all of them will be consider at the same time to see how is the plant. The figure 3.42 represents it with the conditions listed in table 3.10 for continuous conduction mode:

Parameter	Worst case	Considered value
D	Maximum	0.9
I_L	Minimum	1 A
$R_{eq,2}$	Maximum	$10 \cdot \frac{V_{MPP}}{I_{MPP}}$ [8]
V_1-V_2	Minimum	1 V

Table 3.10. Values of the variables of the transfer function in the worst case.

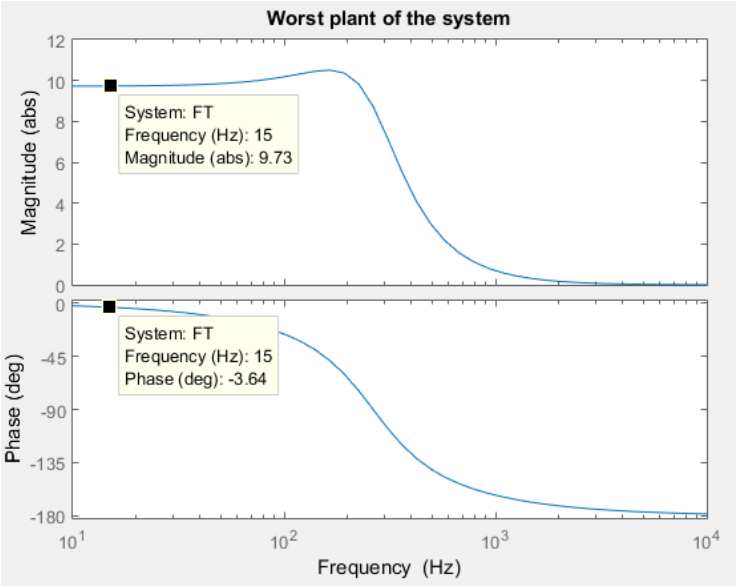

Figure 3.42. Bode diagram of the transfer function of the system.

In the scene represented in figure 3.42, the phase of the system at the working frequency is never below 90 degrees. Thus, a simple integrator with a gain is enough to claim that the steady state error will be eliminated, and the system will be controlled.

The value of the gain determine the cut-off frequency of the loop, and it must be considered that an inner control loop at 60 Hz will be performed by the inverter, which will be considered as a first-order transfer function with a pole at 60 Hz.

With all those considerations, and for a cut-off frequency of 15 Hz, the suitable controller results $G_C = \frac{9.985}{s}$.

Now, both double loops need to be tested working together with different simulations.

For them, typical conditions have been set up as shown in table 3.11:

Parameter	Value
V_1 reference	$V_{MPP,1}$ = 654 V
V_2 reference	$V_{MPP,2}$ = 621.3 V
Initial voltage capacitor 1	$V_{OC,1}$ = 834 V
Initial voltage capacitor 2	$V_{OC,2}$ = 792.3 V
Initial voltage output capacitor	¿?

Table 3.11. Typical values for the references and initial voltage of the capacitors.

The response of the system to the control in the first miliseconds changes considerably depending on the state of charge of the output capacitor (DC bus capacitor of the inverter) at the beginning of the simulation, which can lead to overvoltage in the semiconductors. There is no doubt that, considering that the system initializes in the morning when the sun rises up, the photovoltaic strings will be in open-circuit and therefore their capacitors will have their open-circuit voltage.

However, the value of the DC bus voltage of the three-phase inverter in the start-up is not that clear. Considering that the three-phase inverter works as a three-phase diode bridge, the voltage of the DC bus will be the corresponding rectified voltage from the grid. In this project, the analysed systems are typically connected to low-voltage grid with a root mean square value of 400 V (Europe), so that 560 V are obtained in the DC bus.

The system has been tested with different initial voltages for the DC Bus of the inverter, and the best results appear when the voltage is slightly higher than the initial voltage reference of photovoltaic string one. Therefore, it is recommended to make

the inverter regulate its DC bus voltage in order to achieve the optimal value, before the TIBuck starts to operate. As an example, an optimal combination of initial photovoltaic voltage references and initial voltage for the DC bus are: $V_{1,ref,initial}$ = 690V, $V_{2,ref,initial}$ = 590V, and $V_{out,initial}$=710V.

3.5.3.4 Proving MPPT capability

The control loops have shown that they can control effectively the voltages of each photovoltaic string. However, the maximum power point tracking requires to correct the voltage reference of each string several time for seconds. Therefore, the dynamic response of the system still needs to be tested.

For that, it has been simulated with voltage references that change 4 times per second in steps of ±10 V and ramps of ±275 V/s.

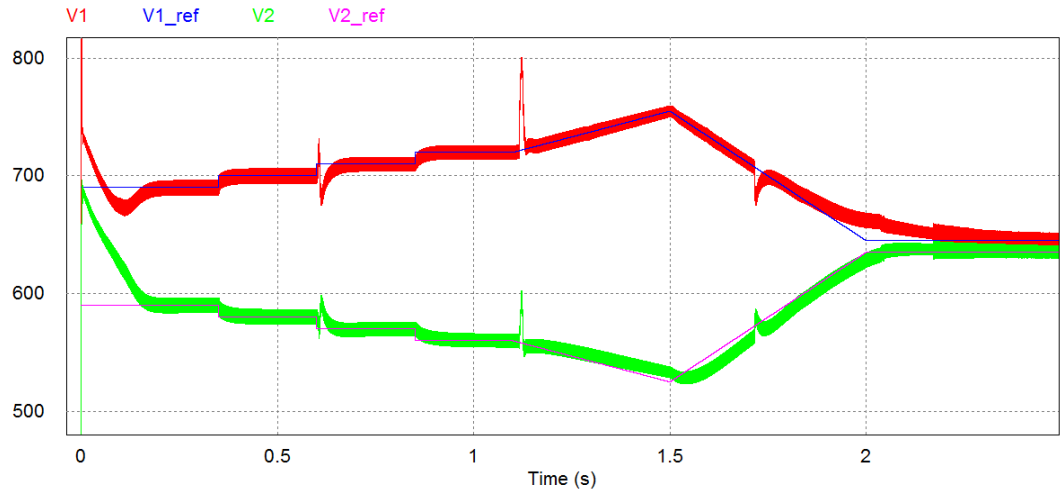

Figure 3.43. Response of the system with the designed control.

The control can deal with the 10 V steps quickly and with no problem, but as the control of V_2 has a lower cut-off frequency, has a delay with bigger changes like the ramp. However, that problem is not important as it is not representative of a real situation, because the MPPT algorithm never provides such big changes for the MPP voltage references. What affects in a more significant way are the overshoots between the reference steps, which seem to be caused by the influence of one control loop to each other.

Furthermore, when references for both input voltages get closer than 15V, the plant of the system changes as the control starts to work in VDCM, and the control is not as effective as it should be. The main reason of this is the instability of the duty cycle that can be observed in the next figure:

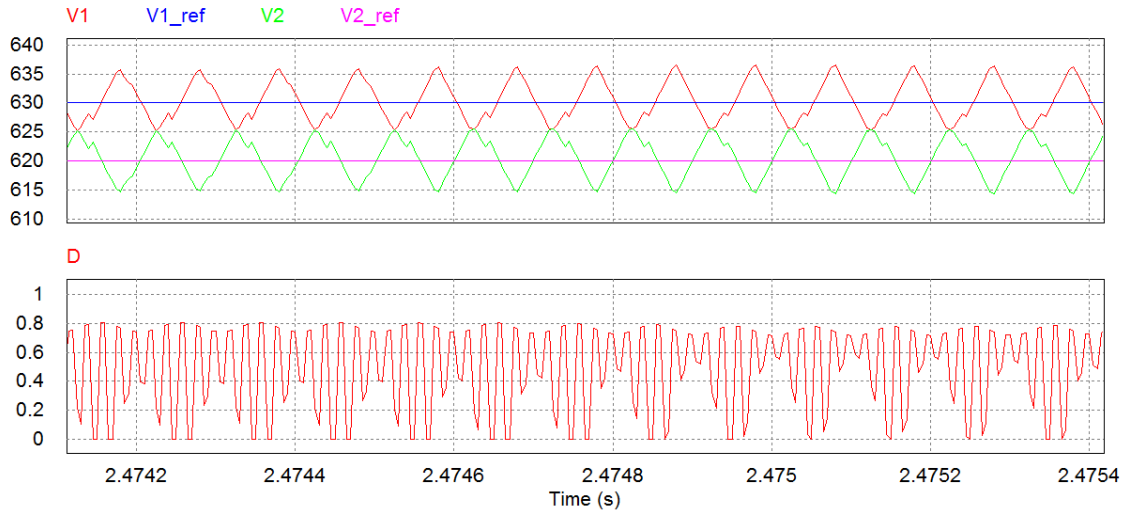

Figure 3.44. Response of the system when voltage references are very close.

Despite the strange waveform of the photovoltaic voltages, their mean values are very close to their references, and the amplitude of their ripples never exceed the limit of 35.77V imposed in chapter 3.4.2.1 to have MPPT losses lower than 0.2%.

Furthermore, as there is one more series photovoltaic module in each string, it will be very hard to find a situation where both values are that close. Nevertheless, the settling time of the response is much higher than in normal conditions, and the mean values of the photovoltaic voltages differ from their references in a few volts.

3.5.3.5 Proposed solution to improve the performance of the control

In other applications where designers decide to put the same number of photovoltaic modules in series in each string, the MPP voltages of both of them would be determined by the mismatch losses. As these losses make the parameters of the module slightly different, the MPP voltages of each photovoltaic string would be very close. In those conditions, the lack of precision in the previous control would affect in a more important way. That situation can also take on importance under partially shaded operation, where both MPP voltage values could get very close randomly.

Furthermore, the voltage peaks that appear between the reference steps can compromise the security of the converter, which is more important than anything else. An easy solution is presented in order to eliminate those problems, improving the accuracy and stability of the photovoltaic voltages during MPPT.

As said before, it seems like both voltage controls affect to each other, especially during rapid changes of their references, and the inner current loop does not provide a stable value of the duty cycle in some situations.

Everything points that they are both consequences of the influence of one loop over the other, so that the system cannot be divided into two SISO (Single Input Single Output) subsystems, one for each photovoltaic voltage, since they are not independent. The difference between the cut-off frequencies of both V_1 (50 Hz) and V_2 (15 Hz) loops seems not to be enough to ensure they work decoupled. Furthermore, the theoretical difference between both cut-off frequencies could be altered in reality, invalidating even more the considered assumptions. However, the influence of one loop over each other can be reduced by simply modifying their compensations.

The control of photovoltaic voltage two (V_2) has been designed through a small-signal analysis, without compensations. However, the same cannot be said for the cascaded control loop of V_1, which has various compensations. In this loop, the influence of the control loop of V_2 is mainly produced through the compensations of V_2, which just appear in the inner current loop. Exactly, all the facts converge to the same solution: Eliminating the compensations of V_2 in the inner current loop to remove the effect of its control loop.

The modified control loop strategy is represented in figure 3.45:

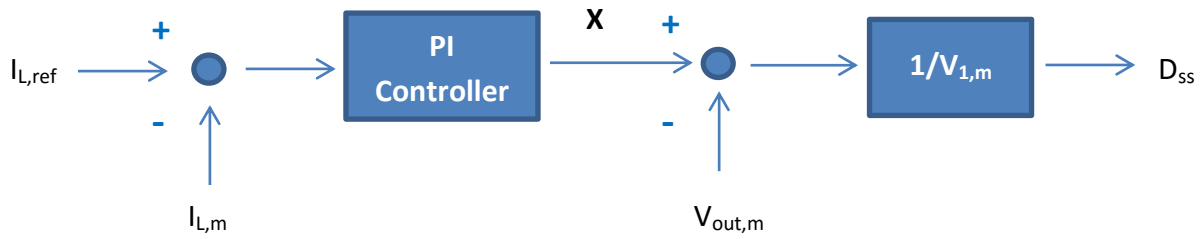

Figure 3.45. Scheme of the inner current loop.

Where $I_{L,ref}$ is the inductor current reference, D_{SS} the steady-state value of the duty cycle, and $V_{out,m}$, $V_{1,m}$ and $I_{L,m}$ the output voltage, the voltage of the PV string one, and the inductor current measurements respectively. Comparing figures 3.45 and 3.34, one notice that the term V_2 has been removed from all the compensations. In that case, the PI controller calculates X= $v_L - v_2 \cdot (1-d)$.

Using the same PI controller than in the previous loop, the performance of the control changes as shown in the next image:

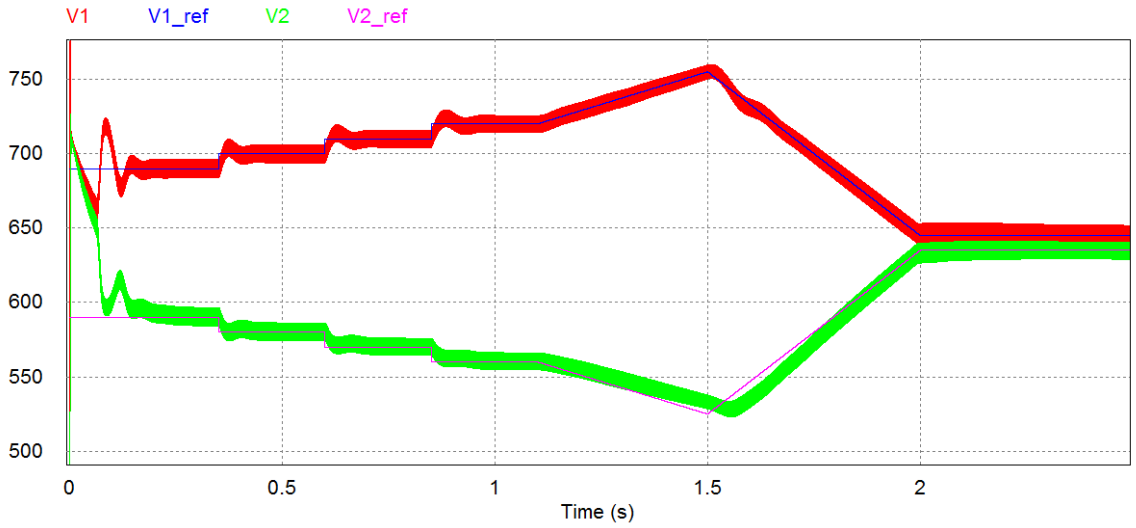

Figure 3.46. Response of the system with the modified control.

The dependence of one control on the other has been removed, making the performance of the whole control a lot better than before. The overshoots between the reference steps disappear, while the difficulties of V_2 following the big ramp persist; it confirms that the reason is the rapidity of the loop, but as mentioned before, voltage changes like that do not represent a real situation and do not compromise the control.

Furthermore, if one enlarges the zone where the references of the photovoltaic strings get closer than 15V, appreciates that both strings follow their references accurately since the converter works in voltage discontinuous conduction mode (VDCM):

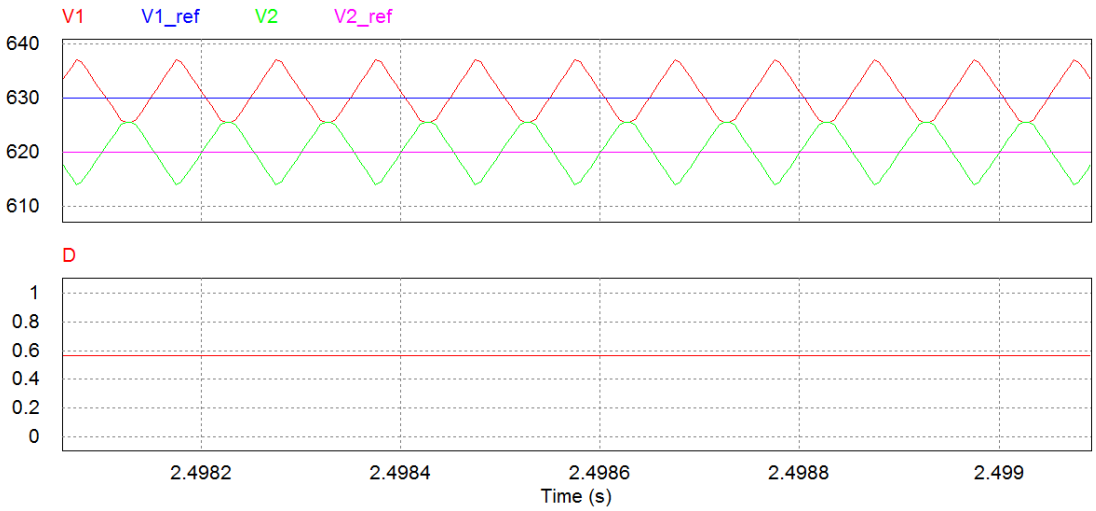

Figure 3.47. Response of the system when voltage references are very close.

The duty cycle does not experiment strange behaviour and reaches a steady-state value with no problem. This happens because the equations for the inner current loop in VDCM, lead to another control loop with the same compensations, since the only term that changes is $v_2 \cdot (1-d) \rightarrow v_2 \cdot (1-d+d_2)$ and the PI controller takes care of it. Furthermore, as the duty cycle (d) in VDCM is very high, this term has less impact on the control.

However, a small-signal analysis is the best option to fully understand why does the same PI controller work for this modified control, since it was designed for a theoretical system plant of $\frac{1}{L \cdot s}$. However, the plant is not the same, and the small-signal analysis could clarify the relationship between the inductor current and the variable X calculated by the PI controller $G=\frac{i_L}{x}$.

The same three equations 3.53, 3.54 and 3.55 obtained in chapter 3.5.1.3 are the starting point of the analysis:

$$\widehat{v_1} \cdot (Cs + \frac{1}{R_{eq,1}}) = -I_L \cdot \hat{d} - \widehat{i_L} \cdot D \quad (3.77)$$

$$\widehat{v_2} \cdot (Cs + \frac{1}{R_{eq,2}}) = I_L \cdot \hat{d} + \widehat{i_L} \cdot (D-1) \quad (3.78)$$

$$\widehat{i_L} \cdot L \cdot s = \hat{d}(V_1 - V_2) + \widehat{v_2} \cdot (1-D) + \widehat{v_1} \cdot D - \widehat{v_{out}} \quad (3.79)$$

In this modified control loop, the duty cycle $D=\frac{X-V_{out}}{V_1}$. Now the small variation of the duty cycle $\hat{d} = \frac{\partial D}{\partial x} \cdot \hat{x} + \frac{\partial D}{\partial v_{out}} \cdot \widehat{v_{out}} + \frac{\partial D}{\partial v_1} \cdot \widehat{v_1} = \frac{\hat{x} + \widehat{v_{out}}}{V_1} - \frac{X+V_{out}}{V_1^2} \cdot \widehat{v_1}$

Where the DC steady-state values of the variables are capitalised, and the small-signal values are marked with a hat. Substituting $\hat{d}$ in 3.77, 3.78 and 3.79 one gets the new three equations that have to be used for this analysis.

$$\left.\begin{array}{l} \widehat{v_1} = f(\hat{x}, \widehat{i_L}, \widehat{v_{out}}) \\ \widehat{v_2} = f(\widehat{i_L}, \hat{x}, \widehat{v_1}, \widehat{v_{out}}) \\ \widehat{i_L} = f(\widehat{v_2}, \hat{x}, \widehat{v_1}, \widehat{v_{out}}) \end{array}\right\} \text{ And solving them } \left\{\begin{array}{l} \widehat{v_1} = f(\hat{x}, \widehat{v_{out}}) \\ \widehat{v_2} = f(\hat{x}, \widehat{v_{out}}) \\ \boxed{\widehat{i_L} = f(\hat{x}, \widehat{v_{out}})} \end{array}\right.$$

The expression rounded in green is the one that interest for the control:

$$\widehat{i_L} = \hat{x}\frac{\left(V_1(V_2-V_1)\left(Cs+\frac{1}{R_{eq,1}}\right)+I_L D V_1\right)\cdot\left(Cs+\frac{1}{R_{eq,2}}\right)-V_1 I_L(1-D)(Cs+\frac{1}{R_{eq,1}})}{\left[Ls\left(I_L(X+V_{out})-CV_1{}^2 s-\frac{V_1{}^2}{R_{eq,1}}\right)-D\cdot\left(D\cdot V_1{}^2-(V_1-V_2)(X+V_{out})\right)\right]\cdot\left(Cs+\frac{1}{R_{eq,2}}\right)-(1-D)(V_1{}^2(1-D)\left(Cs+\frac{1}{R_{eq,1}}\right)-I_L(X+V_{out}))}$$

$$+ \widehat{v_{out}}\cdot FT_2 \qquad (3.80)$$

Again the result is a complex expression that needs to be evaluated depending on 8 different parameters, namely V_1 , V_2 , D , V_{out} , I_L , $R_{eq,1}$, $R_{eq,2}$ and X. However, most of them are closely related; for example, the shunt resistors of the photovoltaic model $R_{eq,1}$ and $R_{eq,2}$ depend on the operating point in the I-V curve of the strings, thus on V_1 and V_2 . Other example is how the output voltage V_{out} depend on the input voltages (V_1 , V_2) , and the duty cycle D.

Furthermore, not all the combinations of the variables can take place in reality, for example $V_1>V_2$, or D never gets to absolute zero or absolute 1.

Therefore, it is clear that the evaluation of expression 3.80 can be really laborious and difficult. However, an acceptable and faster technique can be used to approximate the worst plant of the system by iterating with the different parameters separately, but considering the relationships between them. With that methodology, the worst plant (the one that has the lowest phase margin and the highest cut-off frequency) take place with the values represented in table 3.12:

Parameter	Worst Case	Value
V_1	Maximum	834 V
V_2	Nominal	621.3 V
$R_{eq,1}$	Depends on V_1 → Minimum	$\frac{V_{MPP1}}{10\cdot I_{MPP1}}$ = 3.25 Ω
$R_{eq,2}$	Depends on V_2 → Nominal	$\frac{V_{MPP2}}{I_{MPP2}}$= 30.91 Ω
D	0.4	0.4
V_{out}	Depends on V_1,V_2 and D	$V_2 + (V_1-V_2)\cdot D$=706.38 V
I_L	Maximum	53.2 A
X	Depends on V_2 and D	$-V_2\cdot(1-D)$= -372.78 V

Table 3.12. Values of the different parameters for the worst plant.

It can be observed that the steady-state values of the output voltage V_{out} and X were used to make this approximation. Figures 3.48 represents the approximation of the

worst plant of the system using the values exposed in table 3.12, and the plant that was considered to design the PI controller (1/Ls):

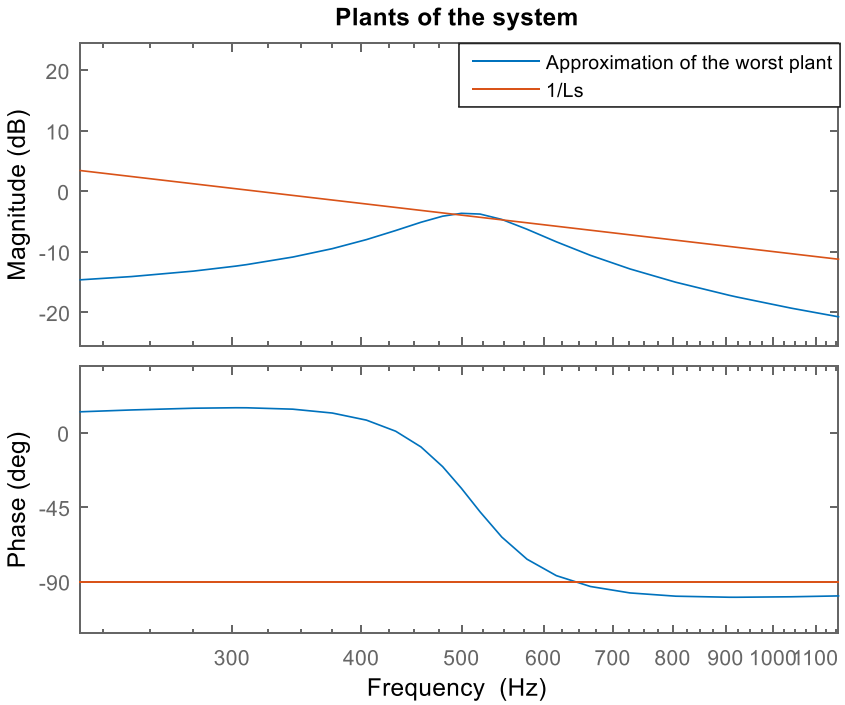

Figure 3.48. Comparison between the real plant and 1/Ls

It can be observed that, at 500 Hz, the magnitude of the worst plant and 1/Ls is almost the same, and the phase is 55 degrees greater than expected. As both plants have almost the same magnitude, the controller work for both of them, but the phase margin when using the modified loop becomes 55 degrees greater than expected in the worst case.

In order to see how the cut-off frequency of the loop changes depending on the operation point of the TIBuck and the photovoltaic arrays, two limiting situations have to be considered. The first of them is represented in table 3.12, and a similar analysis can be done to approximate the other limiting situation, with the lowest cut-off frequency and the highest phase margin. The values of the parameters for that case are exposed in the next table:

Parameter	Worst Case	Value
V_1	Nominal	654 V
V_2	Nominal	621.3 V
$R_{eq,1}$	Depends on V_1 → Nominal	$\frac{V_{MPP1}}{I_{MPP1}}$ = 32.54 Ω
$R_{eq,2}$	Depends on V_2 → Nominal	$\frac{V_{MPP2}}{I_{MPP2}}$= 30.91 Ω
D	0.5	0.5
V_{out}	Depends on V_1,V_2 and D	$V_2 + (V_1-V_2)\cdot D$=637.65 V
I_L	Maximum	53.2 A
X	Depends on V_2 and D	$-V_2\cdot(1-D)$= -310.65 V

Table 3.13. Values of the different parameters for the second limiting plant.

Table 3.13 represents the values of the parameters obtained from the approximation using the same technique that for the other limiting situation. With them the cut-off frequency of the loop is the lowest possible.

The open-loop transfer functions of the system in the two limiting situations, as well as the open-loop transfer function of the system when the plant was 1/Ls, are represented in figure 3.49:

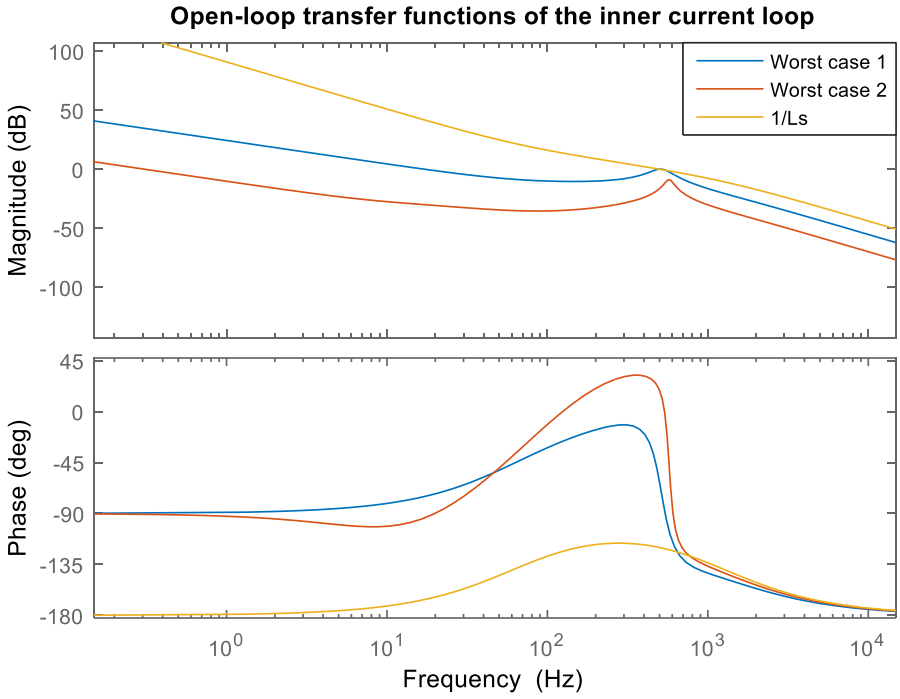

Figure 3.49. Comparison of the cut-off frequencies of the loop depending on the operation point of the TIBuck.

It can be observed that the cut-off frequency of the system can change greatly. However, it can be claimed that it will always be lower than expected, because it will be between the cut-off frequencies of the worst case 1 (around 500 Hz) and worst case 2 (0.15 Hz). However, the system never becomes unstable since the phase margin is large enough, making the control acceptable.

Furthermore, the full cascaded-loop which controls V_1 has been tested for both limiting situations and no problems have been observed. This proves that the big phase margin considered when designing the PI controller of the external voltage loop (60 degrees) can deal with the variations of the phase and magnitude of the inner loop at 50 Hz.

In conclusion, the proposed control strategy can make the converter work in its two most interesting modes depending on the desired photovoltaic voltages, ensuring high dynamic and precise control of the maximum power point voltages, and making the best of the advantages that this converter offers.

Nevertheless, thinking about future working lines for this research, a more rigorous control design considering the converter as a multiple-input multiple-output (MIMO) system should be carried out to ensure that all the influences of the loops are removed.

3.5.4 Adjustment of the control strategy for typical MPPT techniques

The particularities of this new converter could create conflicts when working with typical MPPT techniques that do not consider them. For example, the MPP voltage of string one has to be equal or greater than in string two at all times. Furthermore, the converter is designed to work with a maximum voltage stress in their semiconductors, which is related with the maximum difference between the string voltages.

Those particularities require limits for the difference $V_{1,ref}$ - $V_{2,ref}$, what can be seen as a signal conditioning of the output of the MPPT algorithm, as represented in the next figure:

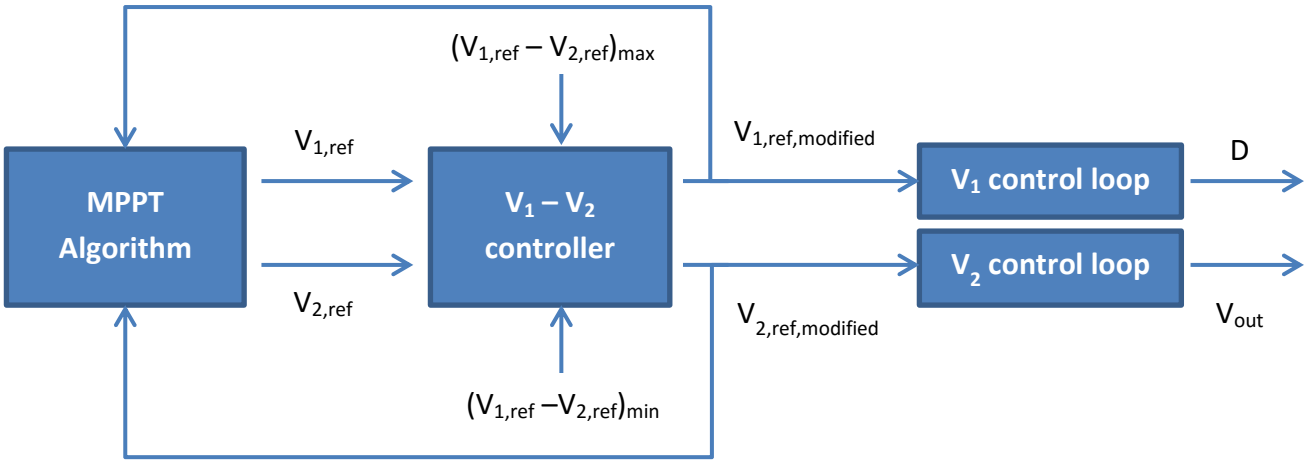

Figure 3.50. Proposed controller of the voltage references.

The two different limits that need to be imposed to the voltage references that come out of the MPPT algorithm will be treated separately in the next sections. However, in case the intermediate V_1-V_2 controller needs to modify any of the voltage references provided by the MPPT algorithm, it has to communicate it to the mentioned algorithm so there is no confusion between them.

3.5.4.1 Lower limit of $V_{1,ref} - V_{2,ref}$

Under partial shading operation of photovoltaic string one, it can happen that its MPP voltage becomes lower than the MPP voltage in string two. This situation cannot take place in this converter as it only uses two-segment semiconductors, allowing to work only with $V_1 \geq V_2$. Thus, the references that come from the MPPT algorithm have to be controlled and changed when needed.

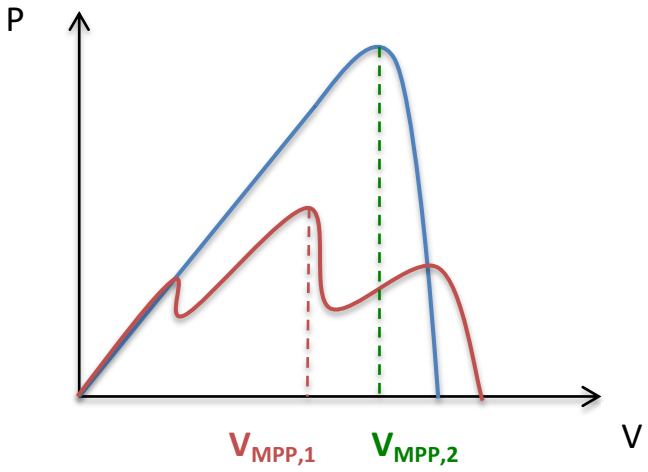

Figure 3.51. P-V curves when $V_{MPP,1} - V_{MPP,2}$ is minimum.

Figure 3.49 shows the P-V curves of the photovoltaic strings for a typical case when V_{MPP1}-V_{MPP2} is minimum, due to partial shading operation of string one.

For those situations, the proposed controller calculates de difference between the voltage references provided by the MPPT algorithm, and compares it with the minimum difference acceptable. In case V_1-V_2 exceeds the minimum, the control changes $V_{1,ref}$, since V_2 is in its absolute maximum power point and is preferred not to be modified. Therefore, the proposed control imposes $V_{1,ref}=V_{2,ref}+(V_1-V_2)_{min}$.

For this application, a minimum value of 1 V will be considered to ensure that $V_{1,ref}>V_{2,ref}$, but without compromising the converter when is working with very close voltage reference, in VDCM. The analogue implementation can be made as shown in figure 3.50:

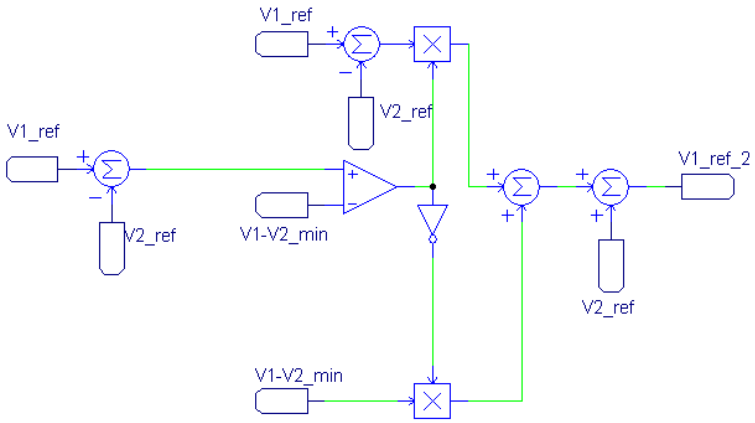

Figure 3.52. Proposed analogue control of $(V_1-V_2)_{min}$

3.5.4.2 Upper limit of $V_{1,ref} - V_{2,ref}$

Along this project, it has been emphasized how important is the value V_1-V_2 for this converter, as is the voltage stress suffered by the semiconductors and determines the size of the inductor.

Controlling this value is essential, but it has been impossible to control the converter through it as demonstrated in chapters 3.5.1 and 3.5.2. High values of V_1-V_2 can appear when the photovoltaic string two is working under partial shading operation, due to a reduction of $V_{MPP,2}$, making the voltage stress of the semiconductors too hard.

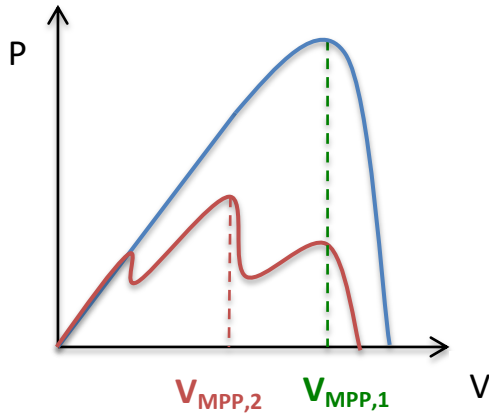

Figure 3.53. P-V curves when V_1-V_2 is maximum.

Figure 3.51 shows a typical case where V_{MPP1}-V_{MPP2} is maximum, due to partial-shading operation of string two.

The proposed controller calculates the difference between the photovoltaic voltage references provided by the MPPT algorithm, and compares it with the maximum difference acceptable. When the difference exceeds the maximum, the controller modifies one of the references in order to accomplish that V_1-V_2 does not exceed the maximum. Photovoltaic array one is presumably generating more power than the array two, so a reduction in the power generated by array two is preferred. Therefore, $V_{2,ref}$ would be limited to $V_{1,ref}$-$(V_1$-$V_2)_{max}$ while V_1 remains unchanged. For this application, a maximum value of 150 V will be considered as the worst case acceptable.

The analogue implementation is represented in the next figure:

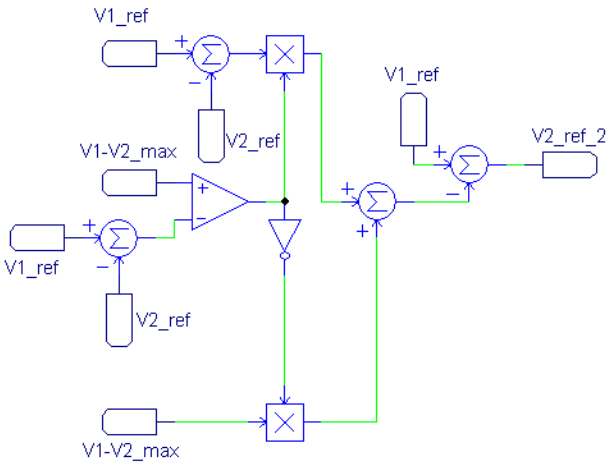

Figure 3.54. Proposed analogue control of $(V_1$-$V_2)_{max}$

3.6 Final Design of the Converter

3.6.1 The inductor

Until the control has not been designed, the main elements of the converter could not be determined, mainly due to the value V_1-V_2. Actually, only the input capacitors of the photovoltaic strings were established with a value of 75 µF based on the maximum MPPT losses admissible, and a commutation frequency of 10 kHz.

Now that V_1-V_2 is controlled, the inductance can be calculated in terms of its current ripple expression 3.37:

$$L = \frac{(V_1 - V_2)_{max}}{4 \cdot \Delta i_{L,max} \cdot F_{com}} = 350\ \mu H$$

Where F_{com} is the commutation frequency (10 kHz) and $\Delta i_{L,max}$ is the maximum current ripple admissible, considered as a 20% of the maximum inductor current possible, which is 53.2 A under STC conditions.

The semiconductors will support a maximum voltage stress of 150 V when the photovoltaic system is working. However, during the night their voltage stress change due to the characteristics of the system:

- The controlled switch S1 is off, so that the photovoltaic string one is isolated and the absence of irradiance makes it behave as a diode with voltage zero.
- The inverter is not working, and it behaves as a three-phase rectifier for the 400 V grid (Europe), providing a DC bus voltage of 565 V.
- The non-controlled switch S2 is off as well, so that the photovoltaic string two does not produce any current and behaves as a diode with voltage zero.

In that situation, both switches support the DC bus voltage of the inverter, which is several times greater than 150 V. Therefore, the semiconductors would need to be oversized to support 560 V, although during operation that value would never exceed 150 V.

In order to avoid that situation and make the most of the converter, a low cost contactor is situated between the inductor and the DC Bus of the inverter to support the 560 V during the night. In particular, the chosen contactor is a KILOVAC LEV100 series contactor from Tyco Electronics®, which supports 900 DC voltage and 100 A DC current [A.3]. For more information, please check the official datasheet attached at the end of this project.

With respect to their current stress, the worst situation would be when all the photovoltaic panels are working under STC conditions, producing a total current at the inductor of 53.2 A.

3.6.2 Semiconductors

A diode is the best choice for a non-controlled switch as it is very commonly used in power electronics, and there are a wide variety of voltages and currents that they support. On the other hand, the low voltages and currents that both switches support allow using a MOSFET instead of an IGBT for the controlled switch, having the advantages of being faster and more efficient.

In this case, as explained before, the maximum voltage that it needs to support is 150 V. However, a security margin of 50% of the expected value is considered in case short voltage peaks take place during commutations. With all, a 250 V voltage stress would be more than enough for this application.

With respect to the maximum current, as it is a thermal limit, the semiconductor manufacturers typically refer to the root mean square value of the current they products can admit. As each photovoltaic string can generate a maximum current under STC conditions of 26.6 A, and the average current of their parallel capacitors are zero, the current waveforms supported by them will have an average value of 26.6 A.

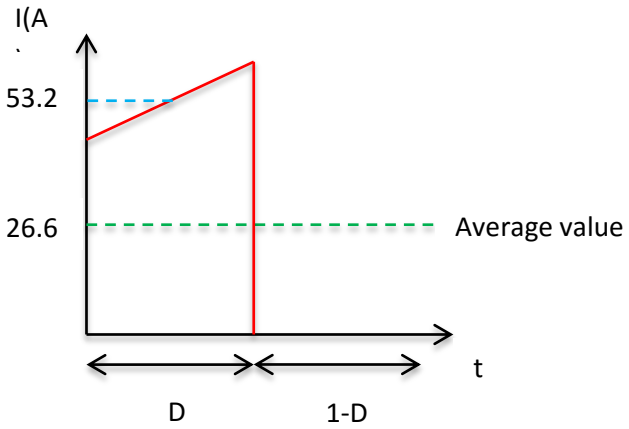

Figure 3.55. Current of the MOSFET in the TIBuck, under STC conditions and with D=0.5.

Figure 3.55 shows the current waveform in the MOSFET or the diode when the converter works with a duty cycle of 0.5. However, different waveforms with different root mean square values can appear with the same average value, depending on the

duty cycle. The highest root mean square value happens with a duty cycle of 0.5 as shown in the previous figure 3.55, making I_{RMS}=37.62 A. In addition, the duty cycle 0.5 is the worst situation for both semiconductors as the same root mean square value is found in them. Therefore, the maximum stress the semiconductors have to support is 150 V and 37.7 A.

The chosen MOSFET is the model IPX200N25N3 G from Infineon® and the diode is the model STTH60P03S from ST®. Their main characteristics are exposed in tables 3.14 and 3.15. For more information, please check the official datasheets attached.

MOSFET	
V_{DS}	250 V
$R_{DS(on),max}$	20 mΩ
$R_{DS(on),typ}$	17.5 mΩ
$I_{D,max,rms}$ (T_c=25ºC)	64 A
$I_{D,max,rms}$ (T_c=100ºC)	46 A

Table 3.14. Main electrical characteristics of the chosen MOSFET. [A.4]

DIODE	
$I_{F(AV)}$	60 A
V_{RRM}	300 V
$V_{FP(TYP)}$	2.5 V
$I_{RM(TYP)}$	6 A
T_j	175 ºC
$V_{F(TYP)}$	0.9 V

Table 3.15. Main electrical characteristics of the chosen diode. [A.5]

4. PERFORMANCE OF THE TWO-INPUT BUCK CONVERTER

In this chapter, the efficiency of the TIBuck will be analysed, and a brief comparison with its current alternative will be made in order to quantify the improvements that this new converter offers. For this study, STC conditions will be considered as it is the nominal working point of the system.

4.1 Efficiency of the TIBuck Converter

This converter will be implemented with a MOSFET from Infineon and a diode from ST, and their datasheets provide different electrical parameters to calculate their losses.

The use of a MOSFET instead of an IGBT with the voltage and current levels mentioned before, make it possible to work with a commutation frequency 40 kHz with no problem, having the advantage of using smaller filters for the measurements. The required value of input capacitors and inductor would be reduced proportionally as well, as shown in equations 3.33 and 3.35, making the required inductance 16 times smaller than the one used in each of the Boosts that the TIBuck substitutes.

With all these, it is decided to analyse the losses of the converter considering both commutation frequencies, and then take a decision after comparing them.

4.1.1 Situation 1. Normal conditions for both PV strings.

In the contemplated situation, both strings work under STC conditions and without shades, so that both strings operate with their MPP voltages and currents. As having said before, in the first input of the converter three strings of 20 series modules are located, and in the second input three strings of 19 series modules.

- MOSFET

  The switching losses are calculated following Infineon's official guide, and considering t_{on} and t_{off} as their typical values of 20 ns and 12 ns respectively. With both strings working in STC conditions, the voltage with which the switches commute is only 35.8 V, and the current is the same that the one represented in figure 3.55.

$$P_S=(E_{ON}+E_{OFF})\cdot F_{com}=V_{DS}\cdot I_D\cdot(t_{on}+t_{off})\cdot F_{com} \begin{cases} P_{S,10kHz}=0.607\ W \\ P_{S,40kHz}=2.43\ W \end{cases}$$

For the conduction losses, a duty cycle of 0.5 is considered for the nominal working point under STC conditions, as both switches conduct the same time. The resistance of the MOSFET when is conducting $R_{DS(ON)}$ is taken as its typical value as well, 16 mΩ.

$$P_C=R_{DS(ON)}\cdot I_D^2\cdot D=22.64\ W$$

- Diode

Diodes turn on spontaneously, which make them have only turn-on losses. Again, the typical value for t_{off} (40 ns) is taken from the datasheet to calculate the switching losses:

$$P_S=E_{OFF}\cdot F_{com}=V_{DS}\cdot I_D\cdot t_{off}\cdot F_{com} \begin{cases} P_{S,10kHz}=0.75\ W \\ P_{S,40kHz}=3.05\ W \end{cases}$$

For the conduction losses, ST provides its own-developed equation for this particular diode, so they are calculated using it. Again, a duty cycle of 0.5 is considered to calculate the root mean square value of the current, which results 37.62 A, and an average value of 26.6 A, as represented in figure 3.53.

$$P_C=[0.88\cdot I_{F(AV)}+0.009\cdot I_{F(RMS)}]\cdot(1-D)=11.87\ W$$

In both switches the conduction losses are a lot greater than the switching ones, as expected from the exceptional voltage stress they support.

- Inductor

The inductor required depends on the commutation frequency. For a commutation frequency of 10 kHz, a 350 µH is needed with a typical parasitic resistance of 20 mΩ. For a commutation frequency 4 times higher, an inductance 4 times smaller is required, and its parasitic resistance is estimated as 4 times smaller too.

As the parasitic resistance changes depending on the commutation frequency of the converter, two different losses appear for each case.

$$P_L = R_L \cdot I_{L(RMS)}^2 \begin{cases} P_{L,10kHz} = 56.6\ W \\ P_{L,40kHz} = 14.05\ W \end{cases}$$

In this case, the losses when commuting at 40 kHz are significantly lower and far compensate the difference observed in the switching losses.

Having calculated all the losses of the converter, and considering insignificant the losses of the contactor, the overall efficiency of the converter can be determined:

$$\eta = \frac{P_{Photovoltaic} - P_{Losses}}{P_{Photovoltaic}} \begin{cases} \eta_{10\ kHz} = 99.74\% \\ \eta_{40\ kHz} = 99.86\% \end{cases}$$

The efficiency results outstanding, especially when commuting at 40 kHz. The switching losses are insignificant compared to the conduction losses, due to the small voltage stress of the semiconductors. Thus, the conduction losses are the ones that mainly determine the efficiency of the converter.

4.1.2 Situation 2. Maximum voltage difference between PV strings

In a situation where the difference between both photovoltaic strings is maximum (150V), the voltage stress of the semiconductors would be maximum as well. Therefore, it is interesting to analyse the efficiency of the converter in this context.

However, in practice this circumstance will only take place when photovoltaic string two is shaded or partially shaded, and so the current produced by it and its power would be reduced too.

For this hypothesis, it will be considered that photovoltaic string two produces half its maximum power point current in STC conditions, 13.3 A, half its nominal power, 8.55 kW. The same calculations that in section 4.1.1 are done with the new voltage and current stresses of the semiconductors and with a duty cycle of 0.5.

Again, in the first input of the converter three strings of 20 series modules are located, and in the second input three strings of 19 series modules.

- MOSFET

The same typical values for the switching times are used. The current that the MOSFET commutes drops from 53.2 A to 40 A due to the reduction of the current generated by photovoltaic string two.

$$P_S = V_{DS} \cdot I_D \cdot (t_{on} + t_{off}) \cdot F_{com} \begin{cases} P_{S,10kHz} = 1.92\ W \\ P_{S,40kHz} = 7.68\ W \end{cases}$$

$$P_C = R_{DS(ON)} \cdot I_D^2 \cdot D = 12.8\ W$$

The switching losses increase due to the greater voltage stress, while the conduction losses decrease to the smaller current stress.

- Diode

$$P_S = E_{OFF} \cdot F_{com} = V_{DS} \cdot I_D \cdot t_{off} \cdot F_{com} \begin{cases} P_{S,10kHz} = 2.4\ W \\ P_{S,40kHz} = 9.6\ W \end{cases}$$

For the conduction losses, ST provides its own-developed equation for this particular diode, so they are calculated using it. Again, a duty cycle of 0.5 is considered to calculate the root mean square value of the current, with a value of 28.3 A.

$$P_C = [0.88 \cdot I_{F(AV)} + 0.009 \cdot I_{F(RMS)}] \cdot (1-D) = 5.98\ W$$

Again the same tendency is observed, the switching losses increase and the conduction losses decrease.

- Inductor

The same parasitic resistance of the respective inductors are considered:

$$P_L = R_L \cdot I_{L(RMS)}^2 \begin{cases} P_{L,10kHz} = 32\ W \\ P_{L,40kHz} = 8\ W \end{cases}$$

The losses at the inductor decrease due to the reduction of the inductor current.

Having calculated all the losses, and supposing that the contactor losses are insignificant, the overall efficiency of the converter can be determined. As mentioned before, for calculating it, a reduction of a 50% of the nominal power of the photovoltaic modules in string two will be considered due to the effect of the reduction of the irradiance at them:

$$\eta = \frac{P_{Photovoltaic} - P_{Losses}}{P_{Photovoltaic}} \begin{cases} \eta_{10\ kHz} = 99.79\% \\ \eta_{40\ kHz} = 99.83\% \end{cases}$$

The efficiency of the converter results slightly higher than before when commuting at 10 kHz, and slightly lower than before when commuting at 40 kHz, making the difference between commuting with 10 kHz and 40 kHz very small. This is produced by the reduction of the conduction losses with respect to the photovoltaic power, which make the switching losses have more weight in the total efficiency. Anyway, the efficiency of the converter does not even drop below 99.79%, which means a great performance in any case.

4.1.3 Situation 3. Minimum voltage difference between PV strings.

Along this paper, it has been mentioned many times the importance and benefits of working in VDCM, since the semiconductors and the inductor work with very low voltage stress, leading to a super high efficiency and extremely low current ripple.

In chapter 3.3 only one of the three different distributions was chosen, but actually the other two configurations make the most of the VDCM as have the same number of series modules in each string. In that context, the difference between the MPP voltages of both strings is determined by the mismatch losses of the modules, which is very small. Thus, the small MPP voltage difference would allow the converter working the majority of the time in VDCM.

Therefore, this section will analyse the efficiency of the TIBuck converter when one of those configurations is used, supposing normal weather conditions (no shades or big temperature differences). The difference between MPP voltages could then become between 1 and 5 V, so that 2.5 V will be considered as an example.

The same methodology than in the previous sections 4.1.1 and 4.1.2 is followed, considering STC conditions and a working point with D=0.5.

- MOSFET

The same values for the different parameters than in section 4.1.1 are taken for these calculations, because only the voltage stress changes. In addition, as described in chapter 3.2.3, both the MOSFET and the diode turn off and on respectively without voltage stress, and therefore without producing power losses.

$$P_S = V_{DS} \cdot I_D \cdot t_{on} \cdot F_{com} \begin{cases} P_{S,10kHz} = 0.027 \text{ W} \\ P_{S,40kHz} = 0.11 \text{ W} \end{cases}$$

$$P_C = R_{DS(ON)} \cdot I_D^2 \cdot D = 22.64 \text{ W}$$

The switching losses decrease very much due to the small voltage stress, while the conduction losses remain constant from section 4.1.1, as the current is the same when considering STC conditions with no shades.

- Diode

The same values of the different parameters considered in section 4.1.1 are taken for these calculations. The average and rms values of the current stay constant from chapter 4.1.1, in 26.6 A and 37.6 A respectively.

The diode has no switching losses during the turn off as it is a spontaneous commutation, and the VDCM makes it produce no losses either during its turn on. Therefore, the diode has only conduction losses, and the same expression provided by the manufacturer is used to calculate them:

$$P_C = [0.88 \cdot I_{F(AV)} + 0.009 \cdot I_{F(RMS)}] \cdot (1-D) = 11.87 \text{ W}$$

Again the same tendency is observed; the switching losses decrease very much, while the conduction losses remain constant from section 4.1.1.

- Inductor

The same parasitic resistance of the respective inductors than in the previous chapters are considered:

$$P_L = R_L \cdot I_{L(RMS)}^2 \begin{cases} P_{L,10kHz} = 56.6\ W \\ P_{L,40kHz} = 14.05\ W \end{cases}$$

The losses in the inductor are the same because they depend on the inductor current, which does not change from chapter 4.1.1.

Having calculated all the losses, and supposing that the contactor losses are insignificant, the overall efficiency of the converter can be determined when locating 3 strings of 19 series modules in each input of the converter:

$$\eta = \frac{P_{Photovoltaic} - P_{Losses}}{P_{Photovoltaic}} \begin{cases} \eta_{10\ kHz} = 99.73\% \\ \eta_{40\ kHz} = 99.86\% \end{cases}$$

The switching losses in these conditions still are insignificant, and the total losses are approximately the conduction losses in the inductor and the semiconductors. These losses depend on the current and not on the voltage, so that if the current does not change, these losses do not change as well. As the current stress of the semiconductor and the inductor depend only on the number of parallel strings in each input of the converter, the number of series modules does not change the power losses of the converter.

However, the more series modules that are located in each string, the biggest the power of the system is, and as the losses do not change, the efficiency of the system increases. This explains why the efficiency of the converter results worse than in case of locating 20 series modules in each string. In that situation, the total power of the system becomes 36 kW and the efficiency of the system increase to 99.75% when commuting at 10 kHz, and remains almost constant in 99.86% when commuting at 40 kHz.

As a conclusion, the voltage stress does not affect significantly to the efficiency of the converter as the conduction losses, which depend on the current, are a lot bigger. Therefore, there are not remarkable advantages in terms of efficiency when working in VDCM.

4.1.4 Reflections about the commutation frequency

After analysing the efficiency of the converter under different conditions, it is clear to see that its losses become even lower when commuting at 40 kHz, although switching losses do not change the efficiency of the converter in an important way. Furthermore, the switching frequency is closely related to the current and voltage ripples, which need to be filtered. Thus, when commuting at 40 kHz, the required filters become smaller.

In addition, the required inductor and input capacitors become 4 times smaller than before (see equations 3.35 and 3.36), making the most of the advantages that this converter offers. Finally, the noise produced during the commutations of the semiconductors is eliminated, since humans cannot notice noises at frequencies higher than 20 kHz.

As all are advantages, the TIBuck switching frequency will be established at 40 kHz for this application.

4.2 Efficiency of Two Parallel Boost Converters

As having explained before, the traditional solution to perform more than one MPPT in photovoltaic systems is to add a DC/DC stage with as many parallel Boost converters are MPPTs are wanted. As one single TIBuck can perfom dual MPPT, the natural comparison would be between two parallel Boost converters and one TIBuck converter.

In Boost converters, the voltage stress of the switches is the output voltage of the converter (Which can be several times higher than the input voltage), and the current stress supported is the inductor current.

In case of using two Boost converters to perform dual MPPT in the same system, the photovoltaic panels of both strings would normally been redistributed in order to have lower voltages at the input. A logical distribution will be considered as represented in the next figure:

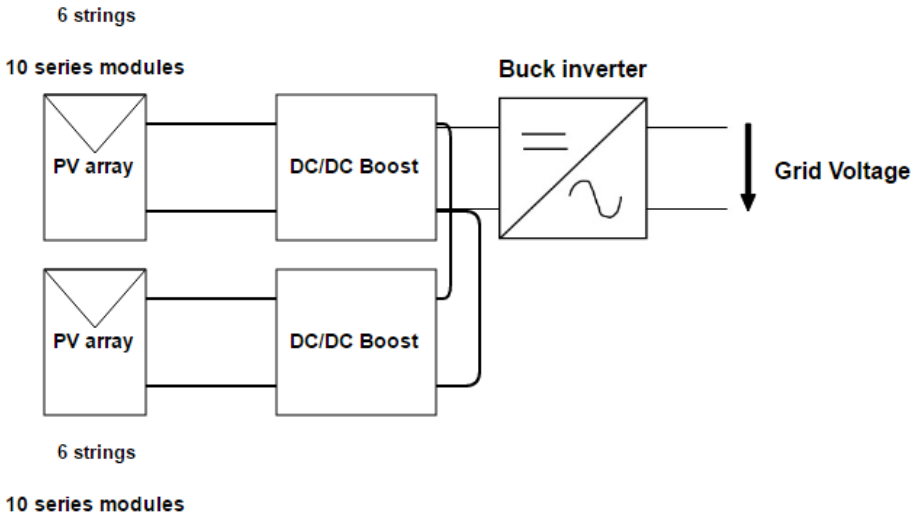

Figure 4.1. Proposed configuration for dual MPPT using two parallel Boost converters.

In this study, STC conditions will be considered as the nominal working point, with a duty cycle of 1/3 in order to have around 600 V in the DC bus of the inverter. In that situation, the controlled switches of each converter would be supporting 600 V and a rms current of 30.7 A, and the non-controlled switches 600V and 43.44 A. Thus, an IGBT instead of a MOSFET and a commutation frequency of 10 kHz are the best choices, according to the current and voltage stresses.

The chosen semiconductors are an IGBT SKM100GAL12T4 from Semikron®, which supports 1200 V and 100 A [A.6], and a diode STTH6012 from ST®, which supports 1200 V and 60 A [A.7]. For further information, please check the official datasheets attached at the end of the project.

With respect to the required inductance of each Boost, an analysis of the inductor voltage leads to the expression $L=\frac{V_{out}\cdot(1-D)\cdot D}{\Delta i_{L,max}\cdot F_{com}}$, where the worst situation takes place with D=0.5. Then, the inductance needed results 1.4 mH.

As a symmetrical distribution of the panels has been considered for this example (the same number of strings and series modules in each input), the efficiency of the two parallel Boost converters is the same than the efficiency of one of them.

- IGBT

In this case, the switching energy figures of the datasheets are used to calculate these losses. As mentioned before, a duty cycle of 1/3 is considered to calculate these losses, and a commutation frequency of 10 kHz:

$E_{ON}(600V,53.2A,r_G=5\Omega)= E_{ON}(600V,100A,r_G=5\Omega) \cdot \frac{53.2}{100}$ = 0.0096 J

$E_{OFF}(600V,53.2A,r_G=5\Omega)= E_{OFF}(600V,100A,r_G=5\Omega) \cdot \frac{53.2}{100}$ = 0.0058 J

$P_S=(E_{ON}+E_{OFF})\cdot F_{com}$= 154.52 W

$P_C=V_{CE(sat),typ}\cdot I_C\cdot D$= 39.01 W

- Diode

Diodes turn on spontaneously and that makes it have only turn-on losses. Again, the typical value for t_{off} is taken from the datasheet. The duty cycle of the MOSFET (1/3) has to be considered for the switching losses.

$P_S=E_{OFF}\cdot F_{com}=V_{DS}\cdot I_D\cdot t_{off}\cdot F_{com}$= 15.96 W

For the conduction losses, ST provides its own-developed equation for this particular diode, so they are calculated using it, considering a duty cycle of (1-1/3) and, according to that duty cycle, an rms current of 43.44 A.

$P_C=[0.88\cdot I_{F(AV)} + 0.009\cdot I_{F(RMS)}]\cdot(1-D)$ = 35.68 W

- Inductor

The inductor required for a maximum current ripple of the 20% of the nominal inductor current (53.2 A), a voltage stress of 600V, and a duty cycle of 1/5 is 1.4 mH. A typical value for its parasitic resistance is 50 mΩ, and the rms value of the inductor current is around 53.2 A, as is almost constant.

$P_L=R_L\cdot I_{L(RMS)}^2$=141.51 W

Considering all the losses, the total efficiency of the DC/DC stage performed by the two Boost inverters would be 97.86%.

4.3 Comparison Between the TIBuck and Two Parallel Boosts

The next table presents the differences between the proposed system and its equivalent using two parallel DC/DC Boost converters:

	Two parallel Boosts	TIBuck	Comparison with two parallel Boosts
Controlled Switch	2x IGBT	1x MOSFET	**Half number of semiconductors**
Non-Controlled Switch	2x Diode	1x Diode	
Maximum Voltage Stress of the semiconductors	600V	150V	**4 times lower**
Maximum Current stress of the semiconductors (RMS)	37.5 A[1]	37.5 A	The same
Switching Frequency	10 kHz	40 kHz	**4 times higher**
Inductance	2x 1.4 mH[2]	1x 87.5 µH	**Half number of inductors. 16 times lower each.**
Efficiency	97.86%	99.86%	**Losses reduced in 15 times**
Flexibility for PV field distribution	High	Limited	**Worse**

Table 4.1. Comparison between two parallel Boosts and one TIBuck.

[1] **Considering the current stress for D=0.5, although with D=0.3 the current stress change for each semiconductor.**
[2] **Considering a maximum duty cycle of D=0.5.**

The comparisons were made considering the conditions and photovoltaic distributions mentioned in sections 4.1 and 4.2.

It is clear that the new TIBuck converter is better than the current option available almost in every aspect. The results are a voltage stress reduction of a 75%, and a required inductance 16 times smaller than the inductance of each Boost when commuting at 40 kHz with the TIBuck and at 10 kHz with the Boosts. That make the converter a lot less bulky, easy to maintain and install, and more robust.

Furthermore, the higher switching frequency of the TIBuck allows using smaller filters to measure the different variables of the converter, and reduces the audible noise as humans cannot perceive noise with a frequency higher than 20 kHz.

The number of semiconductors is reduced in a 50%, and as they support less voltage stress, the economical saving is considerable.

Finally, the new TIBuck converter reduces the thermal losses in 15 times, which take special relevance in medium and high-power systems like the one treated in this project. Consequently, the efficiency of the system gets significantly better: the refrigeration requirements become a lot smaller, reducing the price and maintenance of the converter, while the economical profitability improves.

The only drawback of this converter is the limited freedom when designing the distribution of the photovoltaic strings. This problem has been treated in chapter 3.3, where the limits of the minimum, and especially of the maximum voltage admissible in the DC bus of the inverter, reduced the number of alternatives when choosing the amount of series modules in each string to three: 20/20, 19/19 or 20/19.

The maximum voltage admissible in the DC bus of the inverter is imposed mainly by the module manufacturers, which provide their products with a voltage isolation of 1000 V. However, many of them are actually studying the possibility of increasing that isolation to 1500 V in the following years. If that becomes a reality, the limitations in the design of the photovoltaic strings would be reduced significantly, belittling the main disadvantage that this converter presents.

5. CONCLUSIONS

Along this project, it has been demonstrated that the new TIBuck converter could be a really competitive alternative to Boost converters used in DC/DC stages of medium-power grid-connected photovoltaic systems that are spreading out, now more than ever, in industrial and urban areas, micro-grids, etc. In that context, multiple MPPT are a practical and sometimes required solution where different shade conditions are found in the same photovoltaic system, where different photovoltaic technologies work together (polycrystalline, monocrystalline, etc.), or simply where maximizing the amount of energy generated is the priority.

The new TIBuck represents a great deal, performing dual MPPT effectively with more than 99.85% of efficiency, and using low-cost semiconductors and inductor.

For those situations where a single MPPT is performed through the inverter, this converter offers a worthy of considerable improvement in the energy extracted due to its double MPPT capability, and without almost disrupting the conversion efficiency.

On the other hand, systems which use as many Boost converters as MPPTs are performed, could replace them with half the number of MPPTs of TIBuck converters. In addition, the conversion efficiency would increase significantly while the price and size of the converters are reduced in many times, as proved in table 4.1.

However, the integrated architecture of the converter and the two photovoltaic arrays lead to nonlinearities that complicate the control considerably. The aim of this project was not only to design and study the advantages of the converter, but also to present an effective control of the two photovoltaic voltages in order to perform dual MPPT.

After several attempts, it has been proved that although controlling $\bar{V}=V_{1,ref}-V_{2,ref}$ was very attractive because it represents the voltage stress of the semiconductors and inductor, it is not possible. Therefore, this project proposes a strategy to control the voltages of each photovoltaic array independently, one with each degree of freedom, and makes use of an analogue control to make sure that $\bar{V}$ never exceeds 150 V. The new control is fast enough for medium-power photovoltaic systems, with a dynamic at 50 Hz for photovoltaic array one, and at 15 Hz for the array two. However, when using a commutation frequency of 40 kHz, the dynamic of the photovoltaic array one could be several times quicker

Furthermore, the control results very effective, working successfully in the two most interesting modes of this converter: CCM and VDCM, described in chapters 3.2.1 and 3.2.3 respectively. VDCM is especially attractive for this converter, as the semiconductors and the inductor support very low voltage stress (just a few volts), so that very high efficiency and small current ripple are obtained.

This is why a symmetrical distribution of the photovoltaic modules in the strings could also be very interesting, since the same number of series modules is located in both strings. In that situation, and under normal conditions, the MPP voltages of both strings would be very close and the converter would work in VDCM constantly, taking advantage of all the benefits of this mode.

It has to be mentioned that, in the photovoltaic system, it is required the same number of inverters than TIBucks are wanted to be installed, in order to use the degree of freedom of regulating their DC bus voltages.

Therefore, this converter is specially recommended for those systems that use string-converter architecture (figure 5.1), which is the most common conversion topology in medium and high-power grid-connected photovoltaic systems.

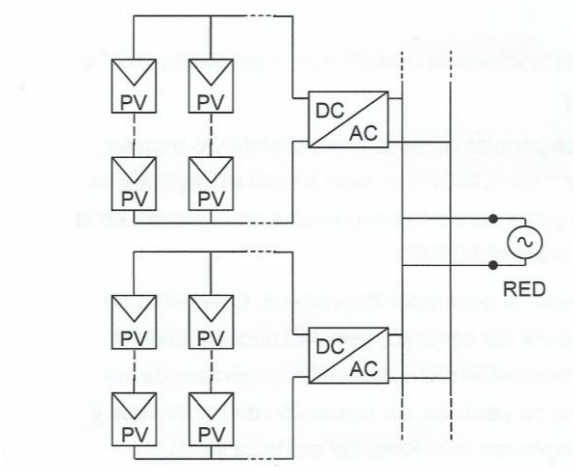

Figure 5.1. String-Converter Architecture [9].

However, the limits of this new converter do not end here, as a lot more research can be done for different power levels, grid or off-grid applications, or even for systems which work with different technologies such as solar photovoltaic and wind power.

With all this, I consider this project a small step forward that can make photovoltaic systems more reliable and cost-competitive with other technologies, supporting ultimately the energy revolution towards a more sustainable word, which I regard necessary in the near future.

6. REFERENCES

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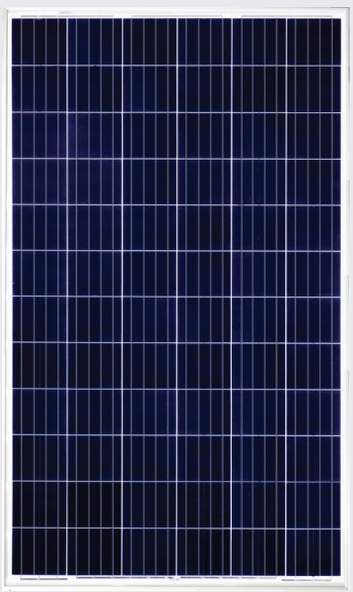
7. ATTACHMENTS

YGE 72 CELL
SERIES 2

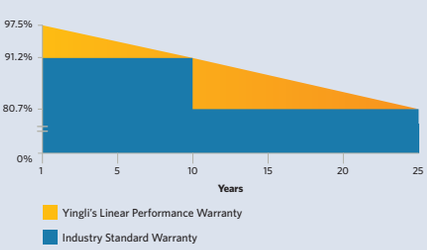


18.5%
CELL EFFICIENCY

10 YEAR
PRODUCT WARRANTY

0 - 5W
POWER TOLERANCE

25 Years Linear Warranty



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PROVEN PERFORMANCE
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Independently tested for proven product quality and long-term reliability. Millions of PV systems installed worldwide demonstrate Yingli's industry leadership.

Durability
Durable PV modules, independently tested for harsh environmental conditions such as exposure to salt mist, ammonia and known PID risk factors.

Advanced Glass
Our high-transmission glass features a unique anti-reflective coating that directs more light on the solar cells, resulting in a higher energy yield.

Extended Size
Our large-format module facilitates system-level cost savings through reduced handling and installation times.

PID Resistant
Tested in accordance to the standard IEC 62804, our PV modules have demonstrated resistance against PID (Potential Induced Degradation), which translates to security for your investment.

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Yingli Green Energy Holding Company Limited (NYSE: YGE), known as "Yingli Solar," is one of the world's leading solar panel manufacturers with the mission to provide affordable green energy for all. Deploying more than 60 million solar panels worldwide, Yingli Solar makes solar power possible for communities everywhere by using our global manufacturing and logistics expertise to address unique local challenges.

YGE 72 CELL SERIES 2

ELECTRICAL PERFORMANCE

Electrical parameters at Standard Test Conditions (STC)

Module type			YLxxxP-35b (xxx=P_{max})					
Power output	P_{max}	W	325	320	315	310	305	300
Power output tolerances	ΔP_{max}	W	0 / + 5					
Module efficiency	η_m	%	16.7	16.5	16.2	16.0	15.7	15.5
Voltage at P_{max}	V_{mpp}	V	37.3	37.0	36.8	36.3	36.1	35.8
Current at P_{max}	I_{mpp}	A	8.72	8.64	8.56	8.53	8.45	8.37
Open-circuit voltage	V_{oc}	V	46.3	46.0	45.7	45.6	45.4	45.2
Short-circuit current	I_{sc}	A	9.24	9.18	9.12	8.99	8.93	8.86

STC: 1000W/m² irradiance, 25°C module temperature, AM1.5g spectrum according to EN 60904-3.
Average relative efficiency reduction of 3.3% at 200W/m² according to EN 60904-1.

Electrical parameters at Nominal Operating Cell Temperature (NOCT)

Power output	P_{max}	W	237.1	233.4	229.8	226.1	222.5	218.8
Voltage at P_{max}	V_{mpp}	V	34.0	33.8	33.6	33.1	32.9	32.7
Current at P_{max}	I_{mpp}	A	6.98	6.91	6.85	6.82	6.76	6.70
Open-circuit voltage	V_{oc}	V	42.8	42.5	42.2	42.1	41.9	41.7
Short-circuit current	I_{sc}	A	7.47	7.42	7.37	7.27	7.22	7.16

NOCT: open-circuit module operation temperature at 800W/m² irradiance, 20°C ambient temperature, 1m/s wind speed.

THERMAL CHARACTERISTICS

Nominal operating cell temperature	NOCT	°C	46 +/- 2
Temperature coefficient of P_{max}	γ	%/°C	-0.42
Temperature coefficient of V_{oc}	β_{Voc}	%/°C	-0.32
Temperature coefficient of I_{sc}	α_{Isc}	%/°C	0.05

OPERATING CONDITIONS

Max. system voltage	1000V_{DC}
Max. series fuse rating	15A
Limiting reverse current	15A
Operating temperature range	-40°C to 85°C
Max. static load, front (e.g., snow)	5400Pa
Max. static load, back (e.g., wind)	2400Pa
Max. hailstone impact (diameter / velocity)	25mm / 23m/s

CONSTRUCTION MATERIALS

Front cover (material / thickness)	low-iron tempered glass / 4.0mm
Cell (quantity / material / dimensions / number of busbars)	72 / multicrystalline silicon / 156mm x 156mm / 3 or 4
Frame (material)	anodized aluminum alloy
Junction box (protection degree)	≥ IP65
Cable (length / cross-sectional area)	1100mm / 4mm²
Plug connector (type / protection degree)	MC4 / IP68 or YT08-1 / IP67 or Amphenol H4 / IP68 or Phoenix Contact SUNCLIX/IP67

• Due to continuous innovation, research and product improvement, the specifications in this product information sheet are subject to change without prior notice. The specifications may deviate slightly and are not guaranteed.
• The data do not refer to a single module and they are not part of the offer, they only serve for comparison to different module types.

QUALIFICATIONS & CERTIFICATES

IEC 61215, IEC 61730, CE, MCS, ISO 9001:2008, ISO 14001:2004, BS OHSAS 18001:2007, PV Cycle, SA 8000

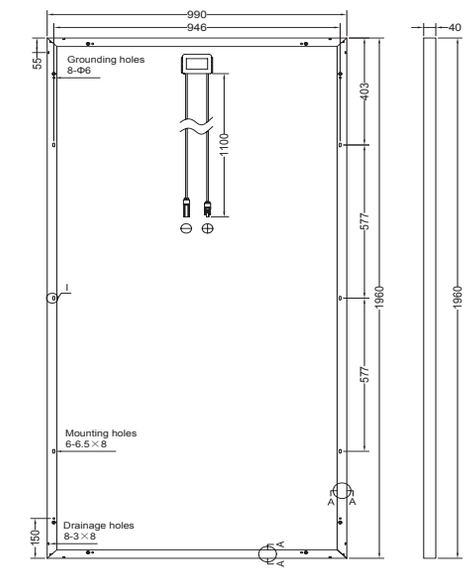
GENERAL CHARACTERISTICS

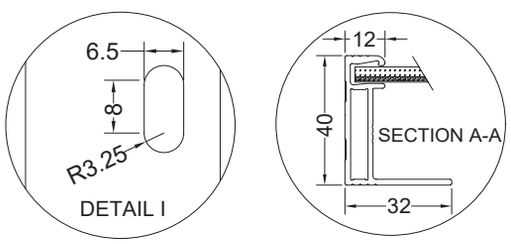
Dimensions (L / W / H)	1960mm / 990mm / 40mm
Weight	25.5kg

PACKAGING SPECIFICATIONS

Number of modules per pallet	26
Number of pallets per 40' container	24
Packaging box dimensions (L / W / H)	1995mm / 1145mm / 1170mm
Box weight	707kg

Unit: mm





Warning: Read the Installation and User Manual in its entirety before handling, installing, and operating Yingli Solar modules.

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A.2

INGECON SUN 3Play
TL Series

10TL / 15TL / 20TL / 28TL / 33TL

THREE-PHASE TL INVERTERS WITH THE MAXIMUM EFFICIENCY AT THE BEST PRICE

A three-phase inverter family for domestic, industrial and large-scale PV plants.

Maximum efficiency at the best price
A single DC-to-AC power conversion stage with an advanced single maximum power point tracking system (MPPT), that makes it possible to harness the maximum energy from the PV array at the most competitive price.

Plug & Play technology
Extremely easy to install. The inverter connection is fast and simple. The country-specific configuration and language can be easily selected from the inverter screen.

Rugged design
Steel casing, especially designed for indoor and outdoor applications (IP65). Able to withstand extreme temperatures. The INGECON® SUN 3Play TL inverters have been designed to guarantee a inverters have been designed to guarantee a long life expectancy, as demonstrated as demonstrated by the stress tests they are subjected to.

Ease of maintenance
Internal datalogger for up to 3 months data storage. Control either from a remote PC or on-site from the inverter front keypad. Status and alarm LED indicators. LCD screen.

Easy to operate
The INGECON® SUN 3Play TL inverters feature a LCD screen for the simple and convenient monitoring of the inverter status and a range of internal variables. The display also includes three LEDs to show the inverter operating status. All this helps to simplify and facilitate maintenance tasks.

Software included
Included at no extra cost are the INGECON® SUN Manager, INGECON® SUN Monitor and its smartphone version Web Monitor for monitoring and recording the inverter data over the internet. RS-485 communications are supplied as standard. In addition, users can download the latest version of the firmware from the Ingeteam website: **www.ingeteam.com,** and update it using a simple SD memory card.

Standard 5 year warranty, extendable for up to 25 years

www.ingeteam.com
solar.energy@ingeteam.com

Ingeteam

10TL / 15TL / 20TL / 28TL / 33TL

Different versions to choose from
In order to satisfy its clients' needs, Ingeteam has created different versions for the INGECON® SUN 3Play TL family:

- "S": Standard version
- "S+": Advanced Standard version
- "P": Premium version
- "P+": Advanced Premium version

All the versions are supplied with DC and AC surge arresters type 3. The "S" version represents the most basic model of all. It features a single MPPT input with terminal blocks. The Advanced Standard version also integrates a DC switch.

On the other hand, the Premium version includes two options for DC connection: conventional terminal blocks or fused and monitored PV connectors.

Moreover, it also features DC fuses, the input current measuring kit and a DC switch. The Advanced Premium version "P+" is supplied with DC surge arresters, type 2.

MAIN FEATURES

- MPPT system.
- 98.5% maximum efficiency.
- Digital inputs.
- RS-485 communications supplied as standard.
- Inverter firmware updating by the user through a SD memory card.
- Software INGECON® SUN Manager for PV plant access and data registration.
- Software INGECON® SUN Monitor for PV plant monitoring.
- LCD display.
- Easy maintenance.
- Display-configurable potential-free contact, to indicate insulation fault or grid connection.
- Plug & Play technology.
- Suitable for indoor and outdoor installations (IP65).
- High temperature performance.
- Different versions to satisfy every project needs.
- Compact design.
- Language, rated voltage and Country Code configurable by display.

PROTECTIONS

- Reverse polarity.
- Shortcircuits and overloads at the output.
- Anti-islanding with automatic disconnection.
- Insulation faults.
- Input and output overvoltages with type 3 surge arresters.

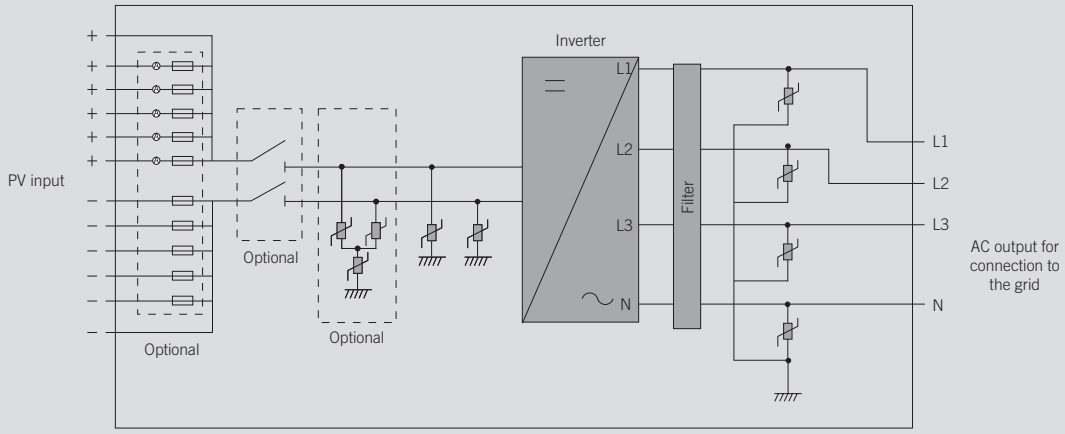
OPTIONAL ACCESORIES

- Inverter communication via Ethernet, GSM / GPRS or Wi-Fi. A second RS-485 communication card is available.
- Self-consumption kit.

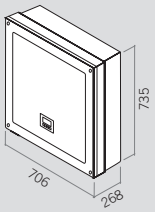
BENEFITS

- The best possible price.
- High efficiency rates.
- Easy maintenance.

3Play TL P+ version (33 kW)



Size and weight (mm)



10TL / 15TL / 20TL
46.8 kg.

28TL / 33TL
51.5 kg.

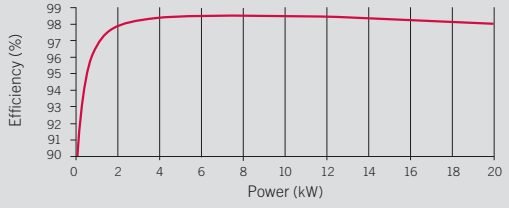
	10TL	15TL	20TL	28TL	33TL
Input (DC)					
Recommended PV array power range[1]	10.3 - 13.4 kW	15.5 - 20.1 kW	20.6 - 26.8 kW	28.9 - 37.5 kW	34 - 45 kW
Voltage range MPP[2]	560 - 820 V				
Min. voltage for Pnom at rated Vac	560 V				
Maximum voltage[3]	1,000 V				
Maximum current[4]	19 A	28 A	37 A	52 A	61 A
Inputs with terminal blocks (Input 1 / Input 2)	1				
Inputs with PV connectors (Input 1 / Input 2)[5]	5	5	5	8	8
MPPT	1				
Output (AC)					
Rated power	10 kW	15 kW	20 kW	28 kW	33 kW
Max. temperature at rated power[6]	55 ºC	55 ºC	55 ºC	51 ºC	51 ºC
Maximum current	15 A	22 A	29 A	41 A	48 A
Rated voltage	400 V				
Voltage range	187 - 528 V	187 - 528 V	187 - 528 V	304 - 528 V	304 - 528 V
Frecuency	50 / 60 Hz				
Power Factor	1				
Power Factor adjustable	Yes. Smax=10 kVA; Qmax=10 kVAR	Yes. Smax=15 kVA; Qmax=15 kVAR	Yes. Smax=20 kVA; Qmax=20 kVAR	Yes. Smax=28 kVA; Qmax=20 kVAR	Yes. Smax=33 kVA; Qmax=20 kVAR
THD	<3%				
Efficiency					
Maximum efficiency	98.5%				
Euroefficiency	98.3%	98.4%	98.3%	98.3%	98.3%
General Information					
Refrigeration system	Forced ventilation				
Air flow	200 m³/h	200 m³/h	200 m³/h	400 m³/h	400 m³/h
Stand-by consumption[7]	10 W				
Consumption at night	1 W				
Ambient temperature	-25 ºC to 65 ºC				
Relative humidity (non-condensing)	0 - 100%				
Protection class	IP65				
Marking	CE				
EMC and security standards	EN 61000-6-1, EN 61000-6-2, EN 61000-6-3, EN 61000-6-4, EN 61000-3-2, EN 61000-3-3, EN 61000-3-11, EN 61000-3-12, EN 62109-1, EN 62109-2, IEC62103, EN 50178, FCC Part 15, AS3100				
Grid connection standards	RD1699/2011, DIN V VDE V 0126-1-1, EN 50438, CEI 0-16 Ed. III, CEI 0-21, VDE-AR-N 4105:2011-08, G59/2, G83/2[8], P.O.12.3, AS4777.2, AS4777.3, IEC 62116, IEC 61727, UNE 206007-1, ABNT NBR 16149, ABNT NBR 16150, South African Grid code, Chilean Grid Code, Romanian Grid Code, Ecuadorian Grid Code, Peruvian Grid code, IEEE 929, Thailand MEA & PEA requirements, DEWA (Dubai) Grid Code, Jordan Grid Code				
Versions available					
Standard version S		✓	✓	✓	✓
Standard version S+		✓	✓	✓	✓
Premium version P	✓	✓	✓	✓	✓
Premium version P+		✓	✓	✓	✓

	Standard version		Premium version	
	S	S+	P	P+
Terminal blocks	✓	✓	✓ (*)	✓ (*)
PV connectors			✓	✓
DC switch		✓	✓	✓
DC surge arresters, type 2				✓
DC and AC surge arresters, type 3	✓	✓	✓	✓
DC fuses			✓	✓
Current measuring kit			✓	✓

(*) Terminal blocks not available for the Premium versions of the INGECON® SUN 28TL and 33TL inverters.

Notes: [1] Depending on the type of installation and geographical location [2] $V_{mpp,min}$ = 560 V when Vac = 400 V. Otherwise: $V_{mpp,min}$ = 1.4 x Vac [3] Must not be exceeded under any circumstances. Consider the voltage increase of the 'Voc' at low temperatures [4] The maximum current per PV connector is 11 A for Premium versions [5] Branch plugs and sockets available to connect two cables to each input [6] For each ºC of increase, the output power will be reduced at the rate of 1.8% [7] Consumption from PV field [8] Related only to inverters up to 16 A.

Efficiency INGECON® SUN 20TL Vdc = 600 V



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A.3

Introducing

KILOVAC LEV100 Series 900 Vdc Contactor

with 1 form X contacts rated 100A continuous

Tyco Electronics

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KILOVAC LEV100 Series 900 Vdc Contactor

PART NUMBERING

Typical Part Number | **LEV100** | **A** | **4** | **A** | **N** | **G**

Series:
LEV100 = 100A Contactor

Contact Arrangement:
A = 1 Form X (SPST-NO-DM)

Coil Voltage:
4 = 12VDC 5 = 24VDC 6 = 48VDC

Coil Wire Length:
A = 15 inches [.4M]

Coil Termination:
N = None – Stripped Wires

Mounting and Power Terminals:
G = Bottom Mount (2 x #8); M5 x 10 H = Side Mount (2 x #8); M5 x 10

NOTE: All part numbers are RoHS compliant.
Specifications are subject to change without notice.

PRODUCT OFFERING

- Bottom Mount Models

3-1618389-7	LEV100A4ANG	12Vdc coil	15”[.4m] leads
9-1618389-8	LEV100A5ANG	24Vdc coil	15”[.4m] leads
3-1618391-7	LEV100A6ANG	48Vdc coil	15”[.4m] leads

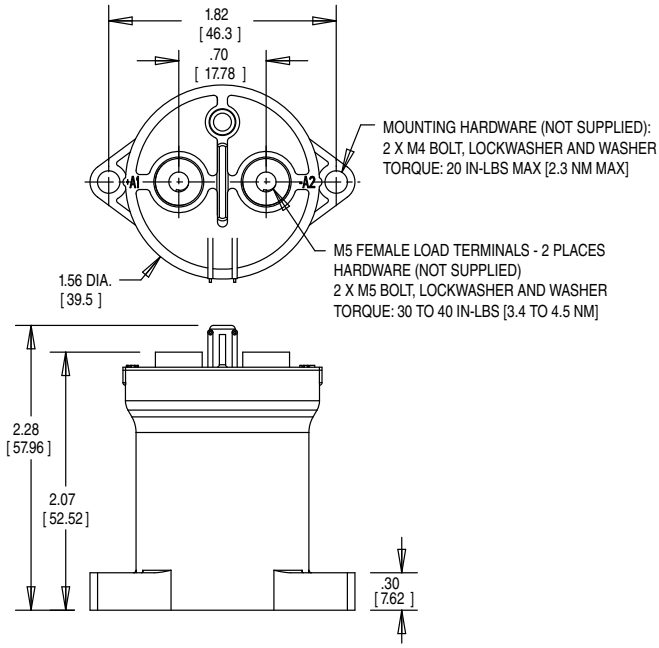
- Side Mount Models

4-1618391-0	LEV100A4ANH	12Vdc coil	15”[.4m] leads
4-1618391-1	LEV100A5ANH	24Vdc coil	15”[.4m] leads
4-1618391-2	LEV100A6ANH	48Vdc coil	15”[.4m] leads

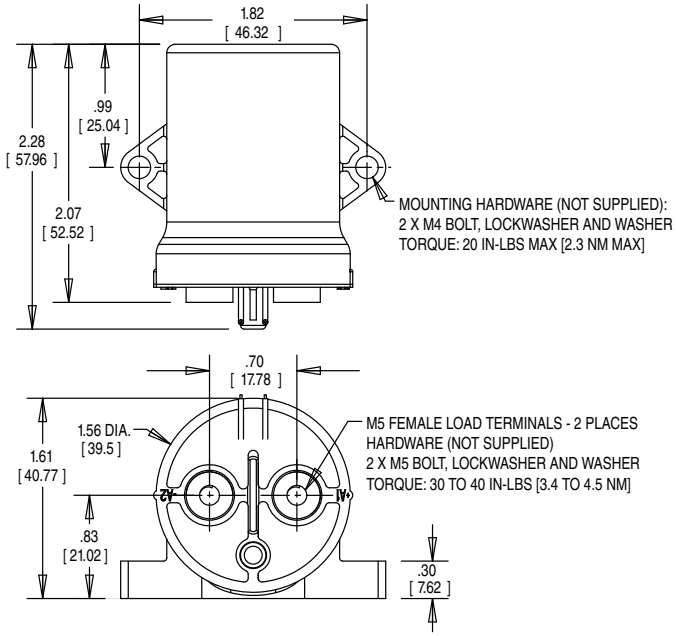
KILOVAC LEV100 Series 900 Vdc Contactor

PERFORMANCE DATA

Bottom Mount



Side Mount



KILOVAC LEV100 Series 900 Vdc Contactor

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KEY FEATURES

Hermetically sealed — intrinsically safe. Operates in explosive/harsh environments without oxidation or contamination of contacts, including long periods of non-operation

8kV isolation between open contacts permits use for high voltage isolation and carry

12, 24 and 48 Vdc coils

Designed and built in accordance to AIAG QS9000

RoHS Ready

DESCRIPTION

Lowest cost, 900 Vdc 100 amp, hermetically sealed DC contactor in the industry

Compact package available in side- or bottom-mount configurations, not position sensitive

APPLICATIONS

Power/motor control circuit isolation, circuit protection and safety in industrial machinery

Automotive battery switching and backup

MECHANICAL

Compact epoxy-sealed resin enclosure occupies only about 4 in^3 (65.5 cm^3)

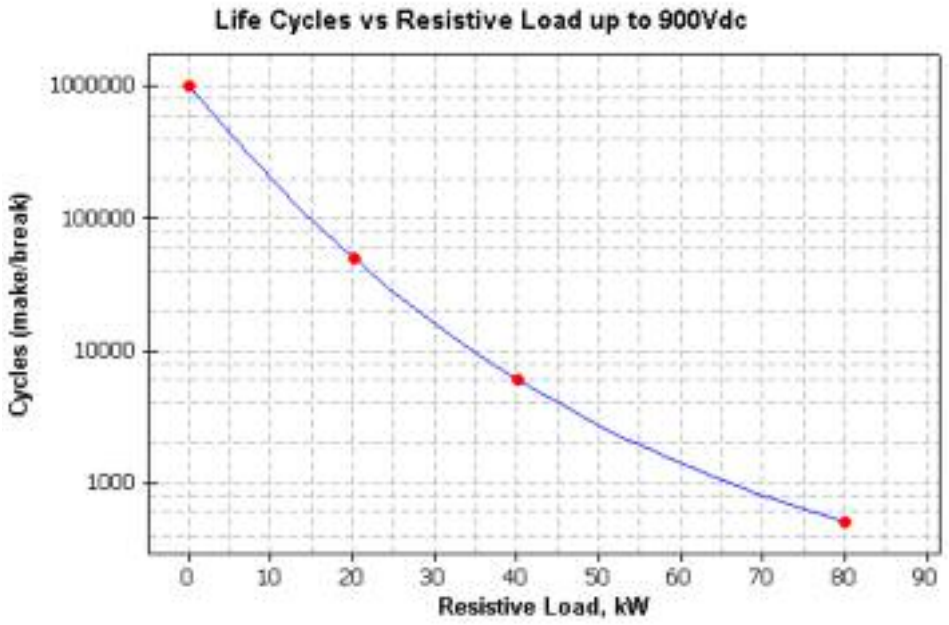
Robust integral mounting plate on either bottom or side of enclosure accepts two M4 screws

Inert gas filled contact chamber

Flying leads for coil connections

Load terminals threaded for M5 bolts (not included)

LOAD LIFE VS. RESISTIVE POWER SWITCHING



PERFORMANCE DATA

Physical Data	
Contact Arrangement: Main Contacts	SPST-NO-DM (1 Form X)
Dimensions	See drawings on page 4
Weight	6.7 oz (190g)

Contact Data	
Contact Arrangement: Main Contacts	SPST-NO-DM (1 Form X)
Voltage Rating: Main Contacts Switching (max)	900VDC
Current Rating: Main Contacts Switching	
Continuous (Note 1)	100A
Short Term -- 3 Minutes (Note 2)	200A
Hot Switching Performance (Polarity sensitive)	
50A make/break @ +400Vdc	50,000 cycles
100A make/break @ +400Vdc	6,000 cycles
100A make/break @ -400Vdc	1,000 cycles
200A make/break @ +400Vdc	500 cycles
1,000A break only @ +400Vdc	25 cycles
600A make only	25 cycles
Maximum Short Circuit Current (1/2 cycle, 60 Hz) (through closed contacts)	1,250A
Dielectric Withstand Voltage (Note 3)	
Between Open Contacts	5,600Vrms/8,000Vdc
Contacts to Coil	2,000Vrms/4,000Vdc
Insulation Resistance, Terminal to Terminal / Terminals to Coil	
When New	100 megohms, min. @ 500Vdc
At End of Life	50 megohms, min. @ 500Vdc
Mechanical Life	1 million cycles

Coil Operating Voltage (valid over temperature range)			
Nominal Voltage	12Vdc	24Vdc	48Vdc
Maximum Voltage	16Vdc	28Vdc	52Vdc
Pick Up Voltage (20°C)	8Vdc	16Vdc	33Vdc
Drop Out Voltage (20°C)	1.2Vdc	2.4Vdc	4.8Vdc
Coil Current (nominal at 20°C, 12vdc)	461mA	250mA	122mA
Coil Power			
Nominal @ Vnom, +20°C	5.5W	6.0W	6.0W
Pickup (close)			
Voltage Max.@85 ° C	9.6Vdc	19.2Vdc	38.4Vdc
Coil Resistance			
Nominal @ +20°C ± 5% (ohms)	26	96	392

Operate & Release Time	
Operate Time Max.	25ms
Operate Bounce Max.	5ms
Release Time	10ms

Environmental Data	
Shock, 11ms 1/2 sine (operating)	20G peak
Sine Vibration, 20G peak	55-2,000 Hz.
Operating Temperature Range	-40°C to +85°C
Noise Emission (at 100 mm distance)	70dB(a)

Notes

Note 1: 8.4 mm^2 conductor. Current rating depends upon conductor size. Keep terminals below 175°C max continuous.

Note 2: 3 minutes at +40°C ambient with 8.4 mm^2 (#8 AWG) conductor.

Note 3: 2,000Vrms minimum under all conditions, until end of life.

FOR MORE INFORMATION

Technical Support

Internet:	www.tycoelectronics.com
E-mail:	newproducts@tycoelectronics.com
USA:	1-800-522-6752
Canada:	1-905-470-4425
Mexico:	1-800-733-8926
C. America:	52-55-1106-0803
South America:	55-11-2103-6000
Hong Kong:	852-2735-1628
Japan:	81-44-844-8013
UK:	44-208-420-8341

Tyco Electronics Corporation
Harrisburg, PA

relays.tycoelectronics.com/kilovac

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A.4

OptiMOS™3 Power-Transistor

Features

- N-channel, normal level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching and synchronous rectification

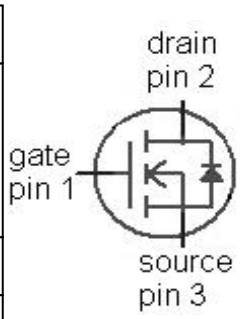
Product Summary

V_{DS}	250	V
$R_{DS(on),max}$	20	mΩ
I_D	64	A

RoHS

Halogen-Free

Type	IPB200N25N3 G	IPP200N25N3 G	IPI200N25N3 G
			
Package	PG-TO263-3	PG-TO220-3	PG-TO262-3
Marking	200N25N	200N25N	200N25N



Maximum ratings, at T_j=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	64	A
		T_C=100 °C	46	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	256	
Avalanche energy, single pulse	E_{AS}	I_D=47 A, R_{GS}=25 Ω	320	mJ
Reverse diode dv/dt	dv/dt		10	kV/µs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	300	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22

[2] See figure 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm2 cooling area[3)]	-	-	40	
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	250	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=270 µA	2	3	4	
Zero gate voltage drain current	I_{DSS}	V_{DS}=200 V, V_{GS}=0 V, T_j=25 °C	-	0.1	1	µA
		V_{DS}=200 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=64 A	-	17.5	20	mΩ
Gate resistance	R_G		-	2.4	-	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=64 A	61	122	-	S

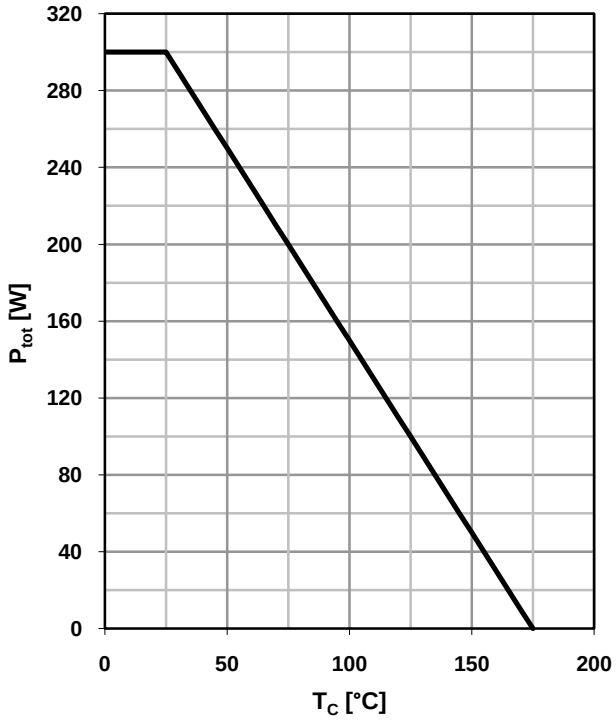
[3)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=100 V, f=1 MHz	-	5340	7100	pF
Output capacitance	C_{oss}		-	297	395	
Reverse transfer capacitance	C_{rss}		-	4	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=100 V, V_{GS}=10 V, I_D=25 A, R_G=1.6 Ω	-	18	-	ns
Rise time	t_r		-	20	-	
Turn-off delay time	$t_{d(off)}$		-	45	-	
Fall time	t_f		-	12	-	
Gate Charge Characteristics[4)]						
Gate to source charge	Q_{gs}	V_{DD}=100 V, I_D=25 A, V_{GS}=0 to 10 V	-	22	-	nC
Gate to drain charge	Q_{gd}		-	7	-	
Switching charge	Q_{sw}		-	13	-	
Gate charge total	Q_g		-	64	86	
Gate plateau voltage	$V_{plateau}$		-	4.2	-	V
Output charge	Q_{oss}	V_{DD}=100 V, V_{GS}=0 V	-	135	179	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	64	A
Diode pulse current	$I_{S,pulse}$		-	-	256	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=64 A, T_j=25 °C	-	1	1.2	V
Reverse recovery time	t_{rr}	V_R=100 V, I_F=25 A, di_F/dt=100 A/µs	-	170	-	ns
Reverse recovery charge	Q_{rr}		-	780	-	nC

[4)] See figure 16 for gate charge parameter definition

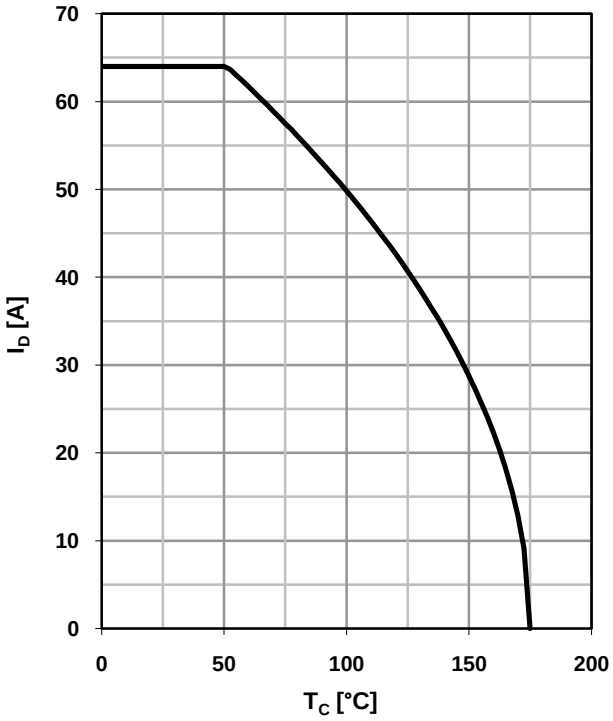
1 Power dissipation

$P_{tot}=f(T_C)$



2 Drain current

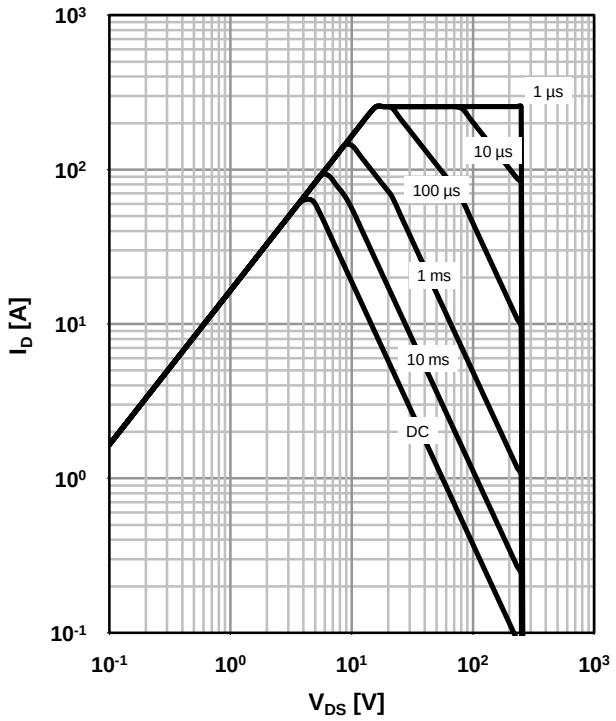
$I_D=f(T_C)$; $V_{GS}\geq 10$ V



3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$

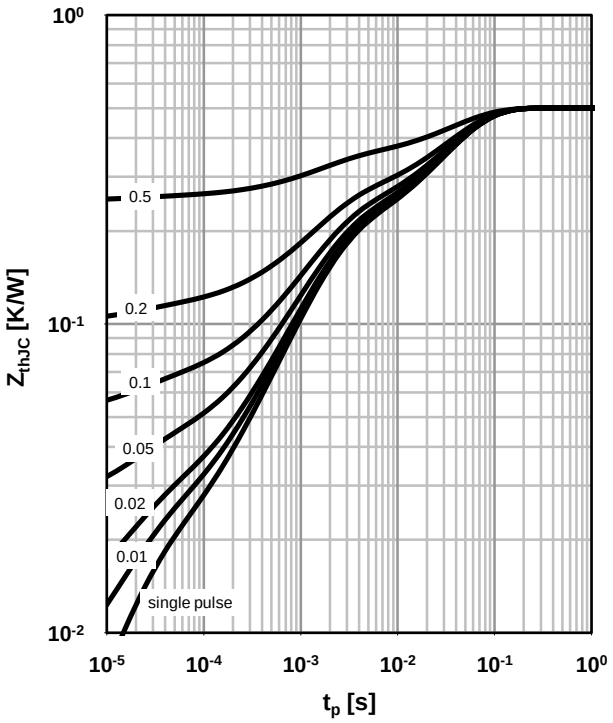
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

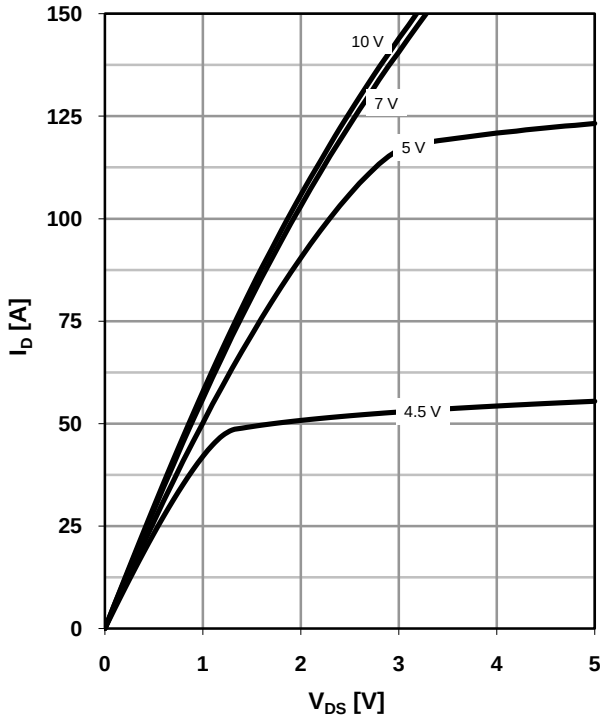
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D=f(V_{DS})$; $T_j=25$ °C

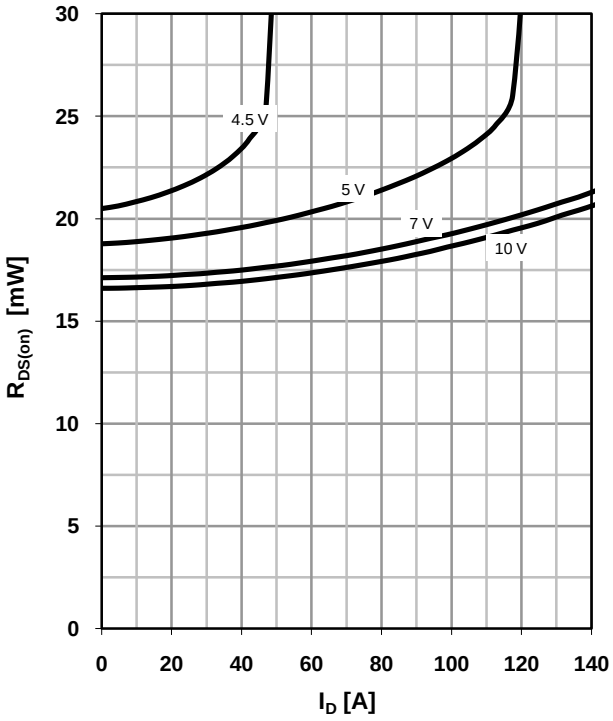
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)}=f(I_D)$; $T_j=25$ °C

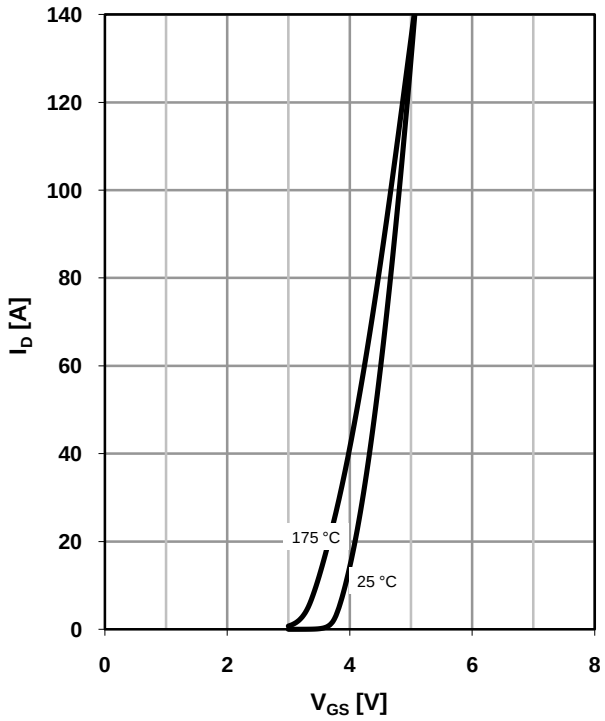
parameter: V_{GS}



7 Typ. transfer characteristics

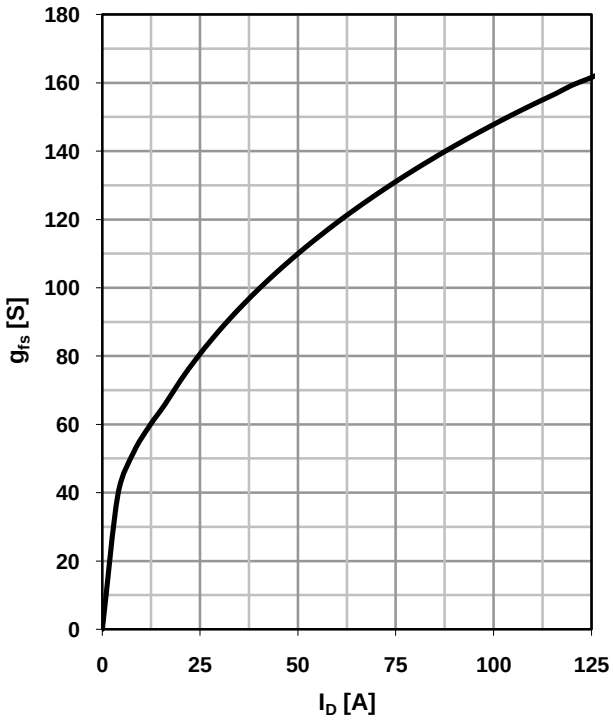
$I_D=f(V_{GS})$; $|V_{DS}|>2|I_D|R_{DS(on)max}$

parameter: T_j



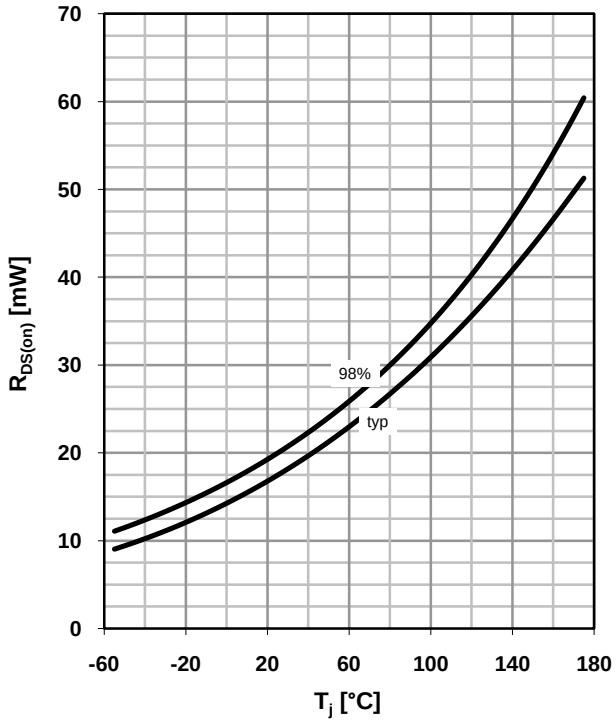
8 Typ. forward transconductance

$g_{fs}=f(I_D)$; $T_j=25$ °C



9 Drain-source on-state resistance

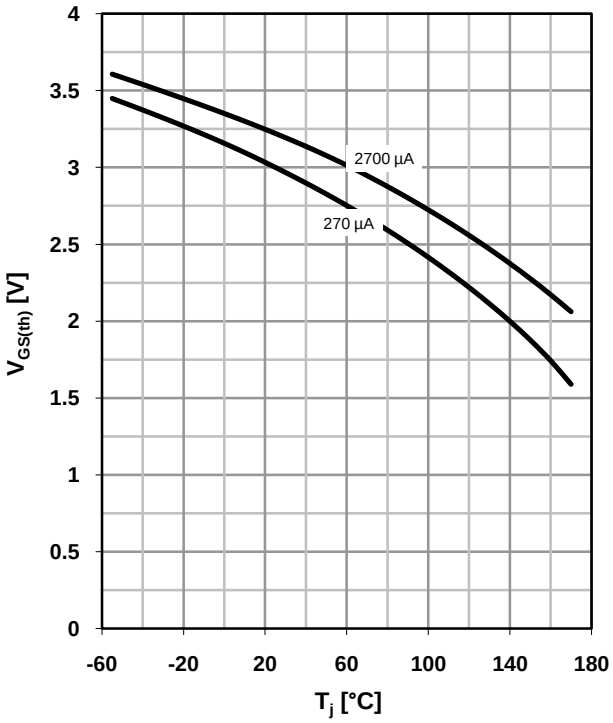
$R_{DS(on)}=f(T_j)$; $I_D=64$ A; $V_{GS}=10$ V



10 Typ. gate threshold voltage

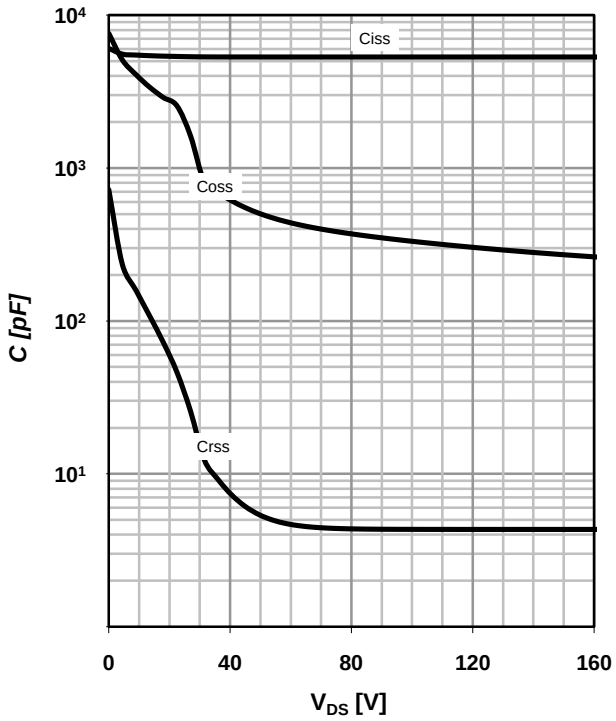
$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$

parameter: I_D



11 Typ. capacitances

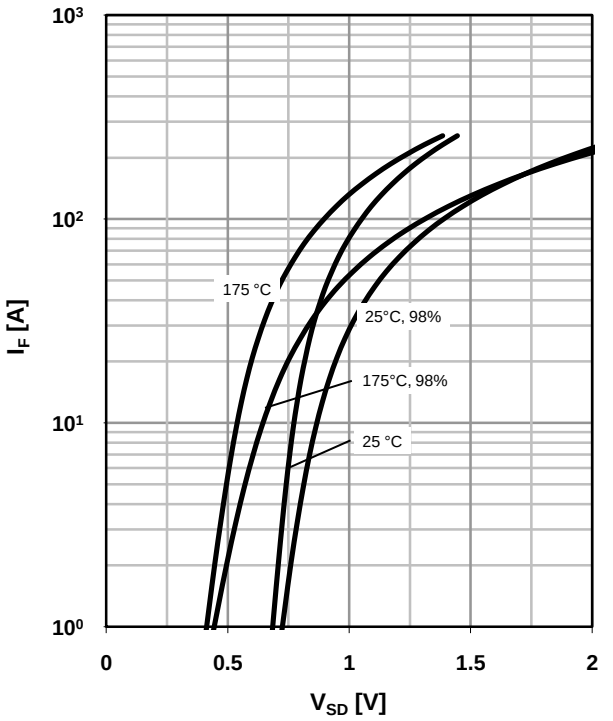
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

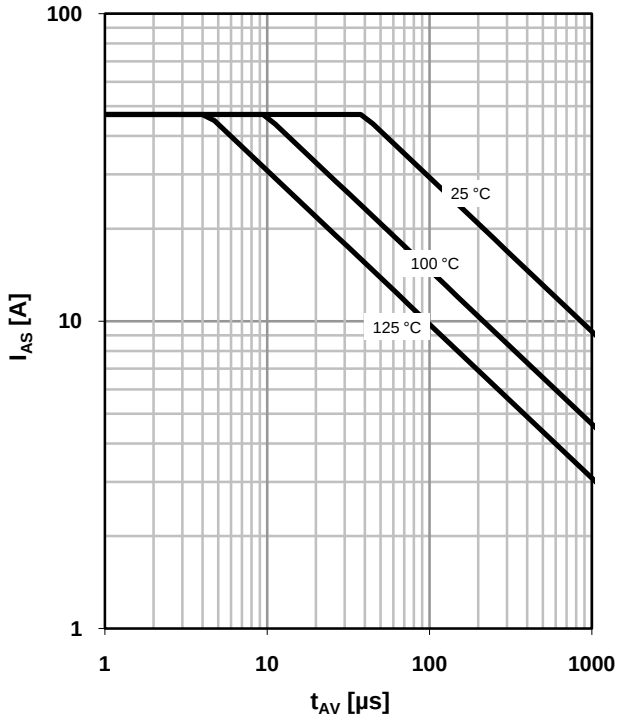
parameter: T_j



13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

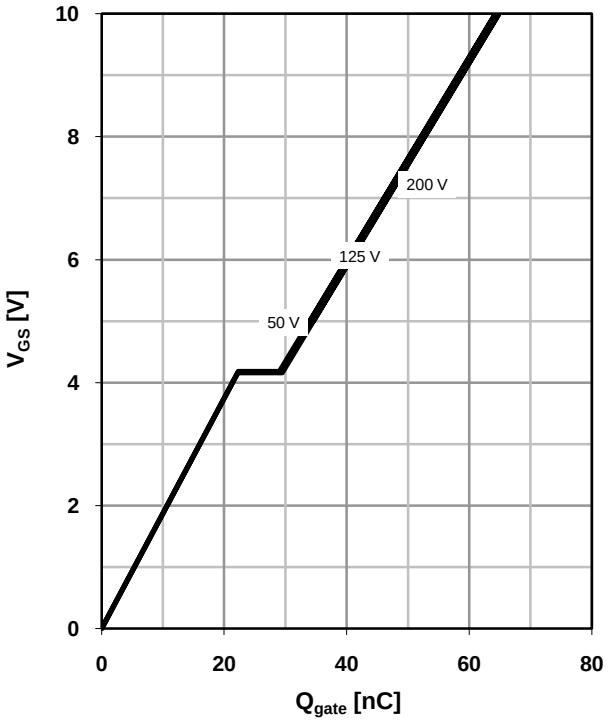
parameter: $T_{j(start)}$



14 Typ. gate charge

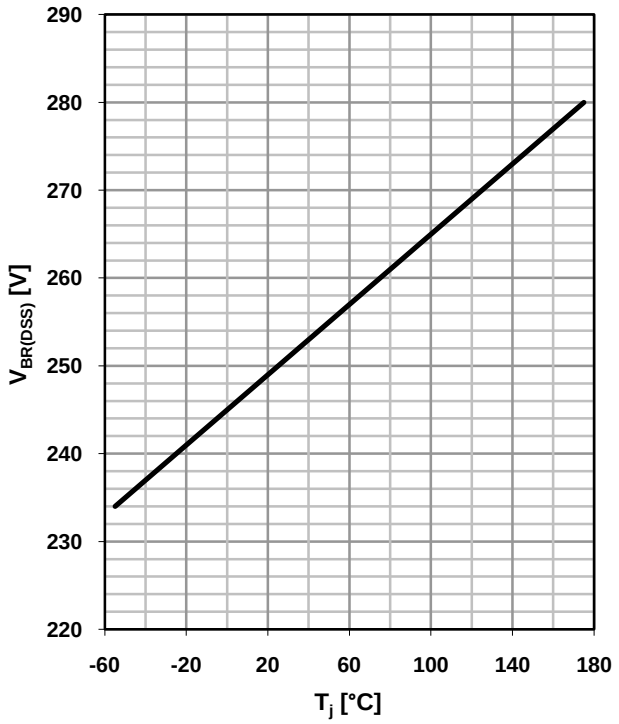
V_{GS}=f(Q_{gate}); I_D=25 A pulsed

parameter: V_{DD}

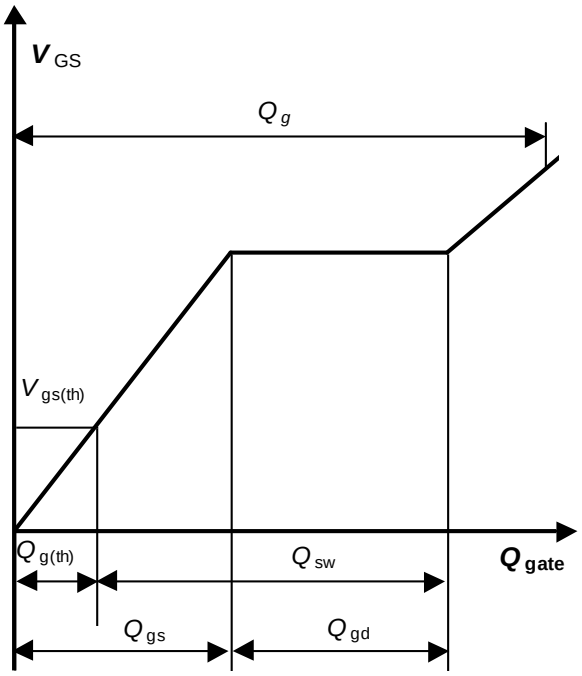


15 Drain-source breakdown voltage

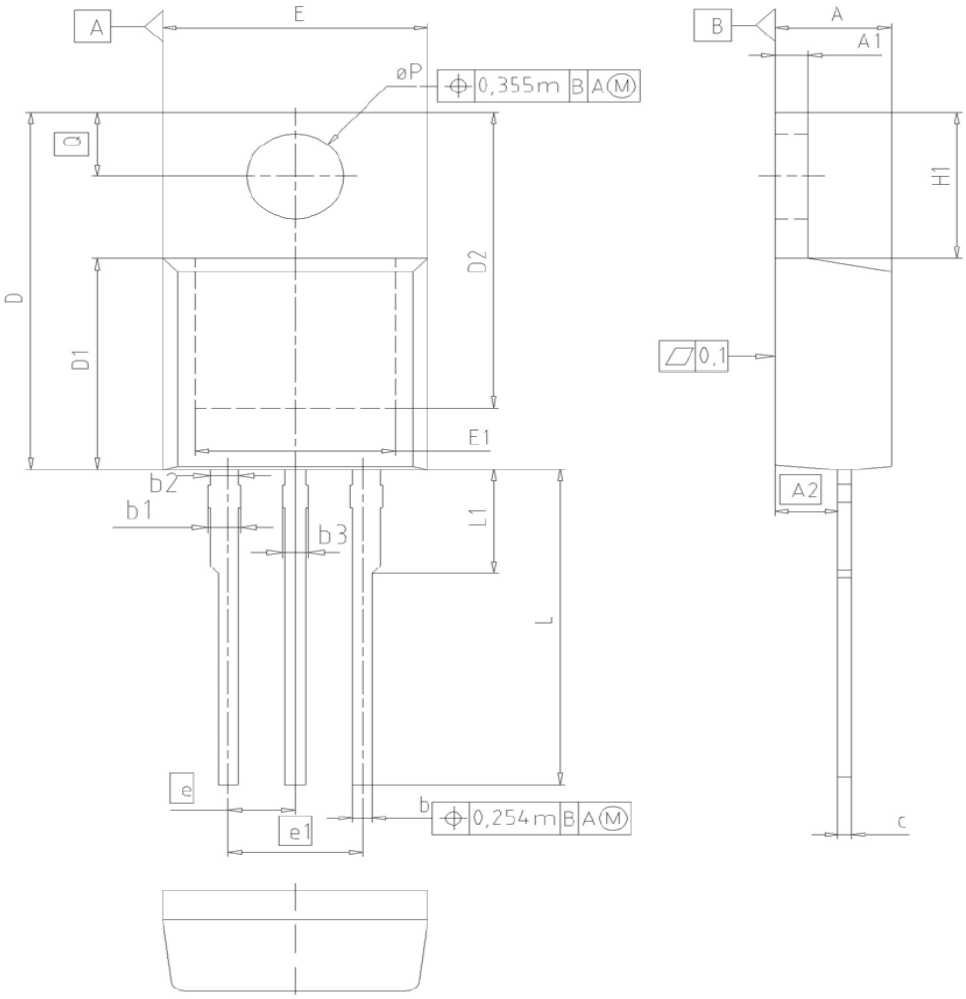
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



16 Gate charge waveforms



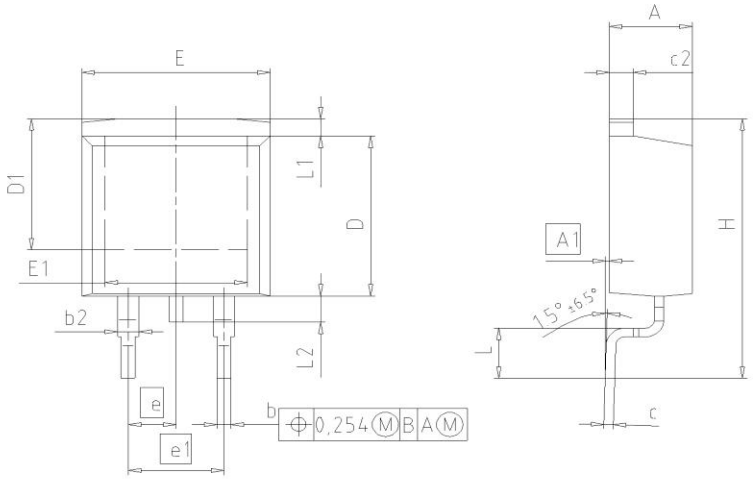
PG-TO220-3: Outline



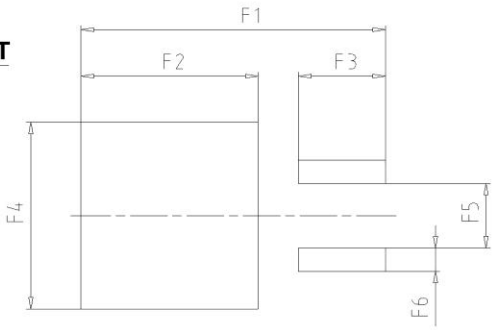
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.	Z8B00003318
SCALE	0, 2.5, 0, 2.5, 5mm
EUROPEAN PROJECTION	
ISSUE DATE	23-08-2007
REVISION	05

PG-TO263-3: Outline



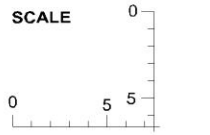
FOOTPRINT



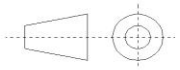
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO.
Z8B00003324

SCALE



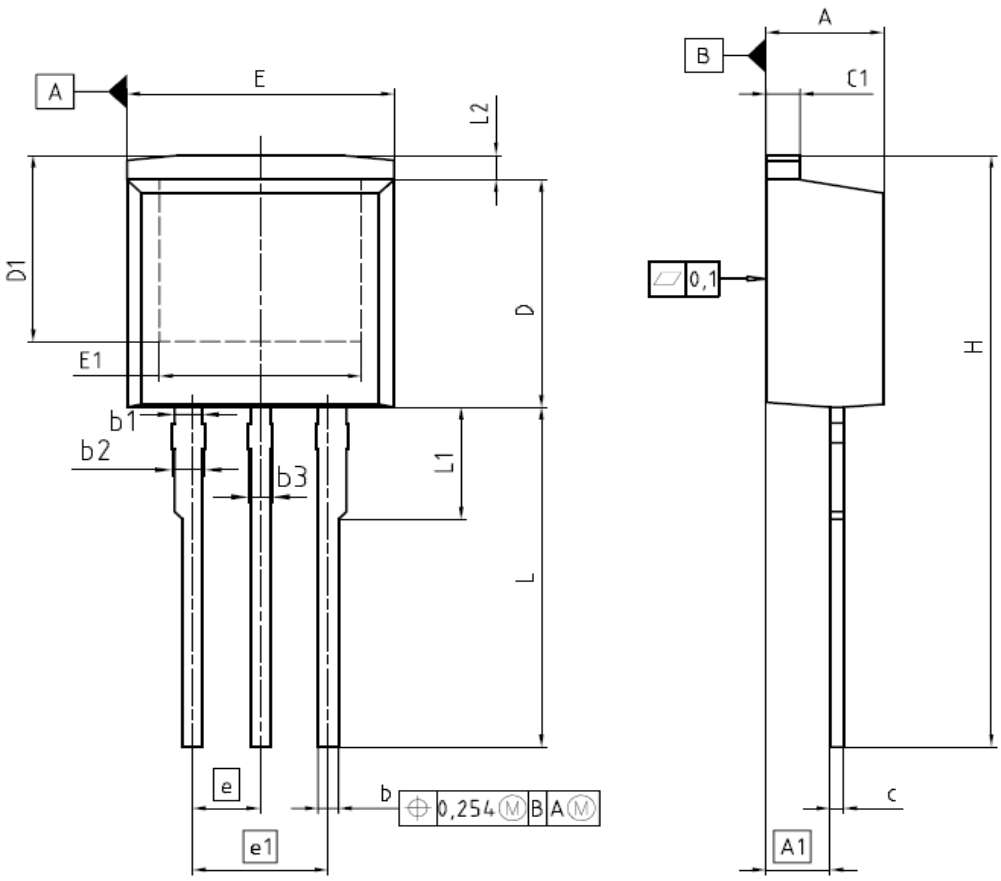
EUROPEAN PROJECTION



ISSUE DATE
30-08-2007

REVISION
01

PG-TO262-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.650	1.118	0.026	0.044
c	0,330	0,600	0,013	0,024
c1	1.170	1.400	0.046	0.055
D	8,509	9,450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6,500	8,600	0,256	0,339
e	2.540		0.100	
e1	5,080		0,200	
N	3		3	
L	13,000	14,000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
Z8B00003325

SCALE
0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

REVISION
03

Published by
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A.5

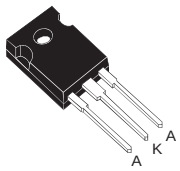
STTH60P03S

Ultrafast rectifier PDP energy recovery

Datasheet – production data

Features

- Ultrafast recovery allowing high sustain frequency
- Decrease charge evacuation time in the inductance
- Minimize switching-on and total power losses
- Increase luminous efficiency and brightness
- Soft and noise-free recovery
- High surge capability
- High junction temperature



TO-247
STTH60P03SW

Description

The STTH60P03SW is an ultrafast recovery power rectifier dedicated to energy recovery in PDP application.

The key parameters of the D_{ERC} diode for the energy recovery circuit have been optimized to decrease power losses.

Table 1. Device summary

Symbol	Value
$I_{F(AV)}$	60 A
V_{RRM}	300 V
V_{FP} (typ)	2.5 V
I_{RM} (typ)	6 A
T_j	175 °C
V_F (typ)	0.9 V

1 Characteristics

Table 2. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		300	V
$I_{F(RMS)}$	Forward rms current		80	A
$I_{F(AV)}$	Average forward current		60	A
I_{FSM}	Surge non repetitive forward current	t_p = 10 ms Sinusoidal	250	A
I_{FRM}	Repetitive peak forward current	F = 200 kHz, t_p = 500 ns Sinusoidal, T_C = 155 °C	150	A
T_{stg}	Storage temperature range		-65 to + 175	°C
T_j	Maximum operating junction temperature		175	°C

Table 3. Thermal parameters

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to case	0.8	°C/W
$Z_{th(j-c)}$	Transient thermal resistance at 1 µs	0.002	°C/W

Table 4. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ	Max.	Unit
I_R (1)	Reverse leakage current	T_j = 25 °C	V_R = 0.7 x V_{RRM}			100	µA
		T_j = 125 °C			0.1	1	mA
V_F (2)	Forward voltage drop	T_j = 25 °C	I_F = 30 A			1.5	V
		T_j = 125 °C			0.9	1.15	

1. Pulse test: t_p = 5 ms, δ < 2%
2. Pulse test: t_p = 380 µs, δ < 2%

To evaluate the conduction losses use the following equation:

$P = 0.88 \times I_{F(AV)} + 0.009\ I_F{}^2{}_{(RMS)}$

Table 5. Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ	Max.	Unit
I_{RM}	Reverse recovery current	T_j = 100 °C	I_F = 60 A, V_R = 100 V dI_F/dt = 200 A/µs		6	7.5	A
S_{factor}	Softness factor				0.5		-
V_{FP}	Peak forward voltage	T_j = 25 °C	I_F = 60 A, dI_F/dt = 400 A/µs		2.5	3.5	V

Figure 1. Forward voltage drop versus forward current

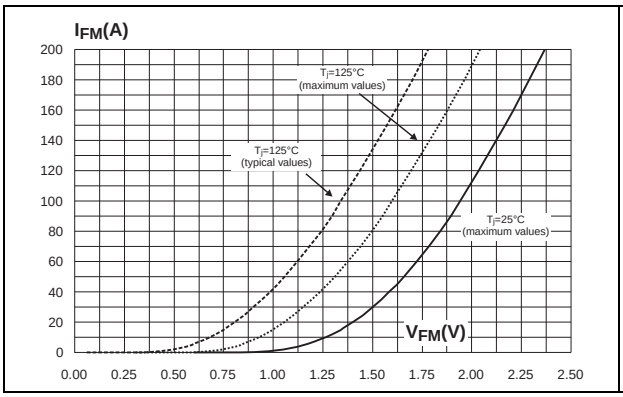


Figure 2. Relative variation of thermal impedance junction to case versus pulse duration

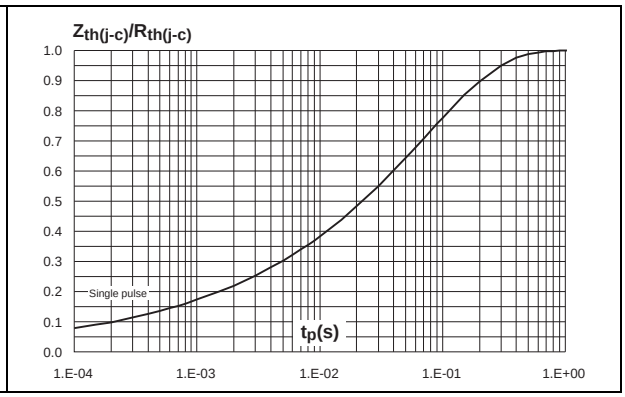


Figure 3. Peak reverse recovery current versus dI_F/dt (typical values)

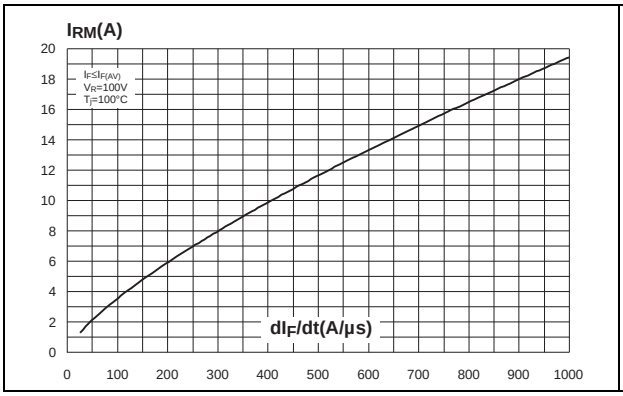


Figure 4. Reverse recovery time versus dI_F/dt (typical values)

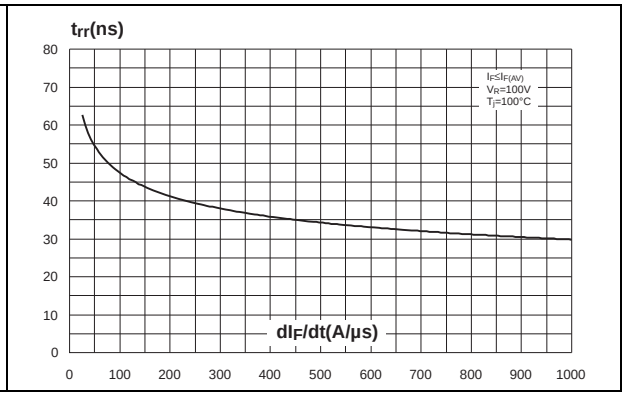


Figure 5. Reverse recovery softness factor versus dI_F/dt (typical values)

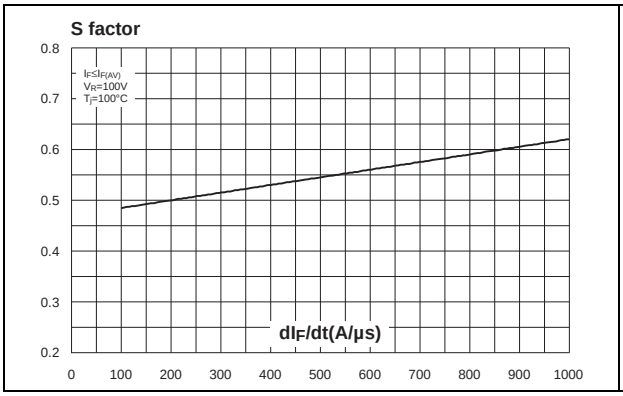


Figure 6. Relative variations of dynamic parameters versus junction temperature

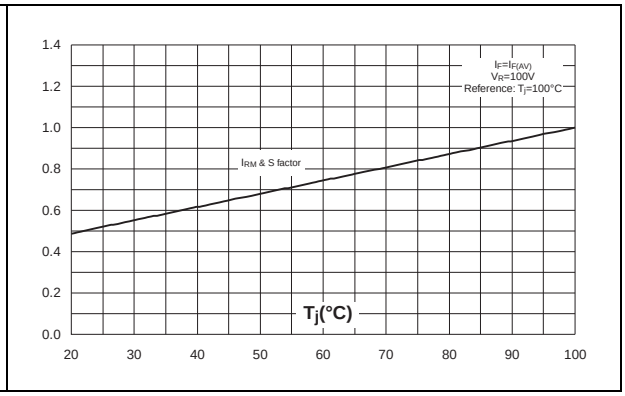


Figure 7. Transient peak forward voltage versus dI_F/dt (typical values)

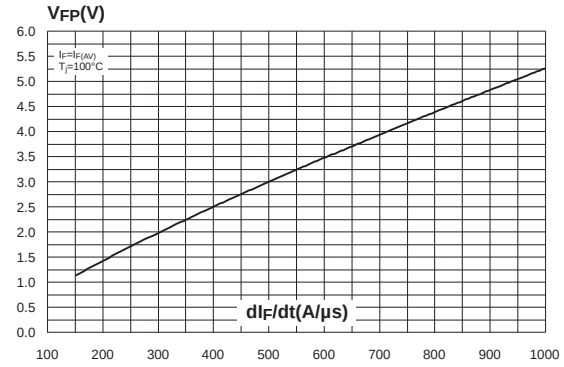


Figure 8. Forward recovery time versus dI_F/dt (typical values)

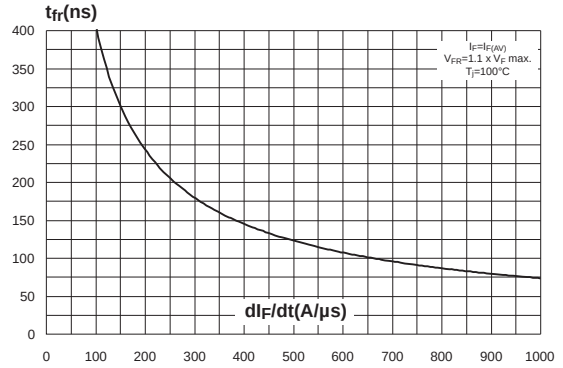
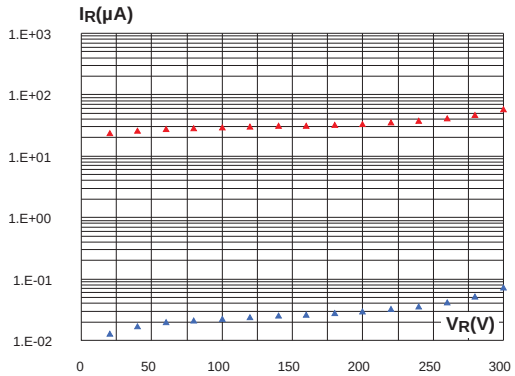


Figure 9. Reverse leakage current versus reverse voltage



2 Application information

Figure 10. Application characteristics

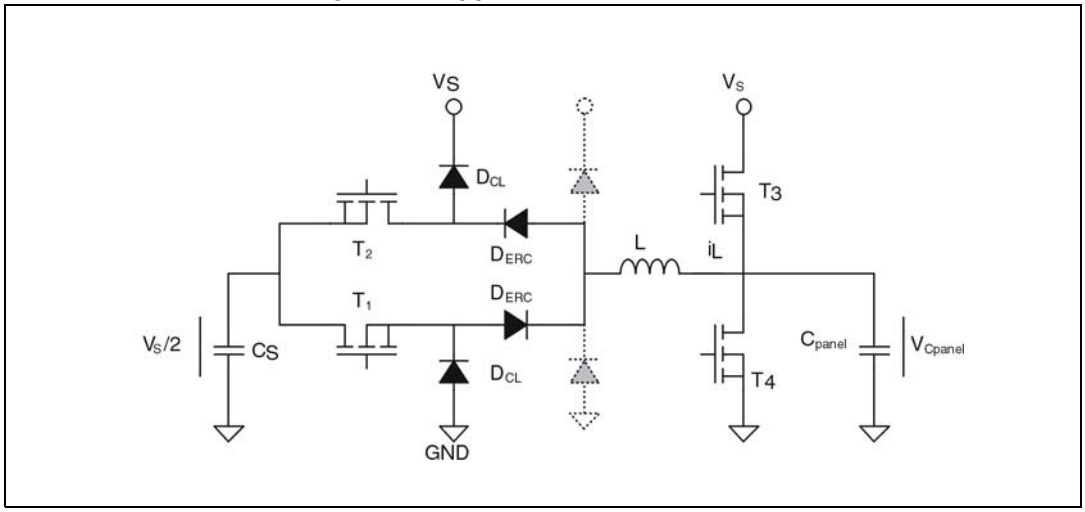
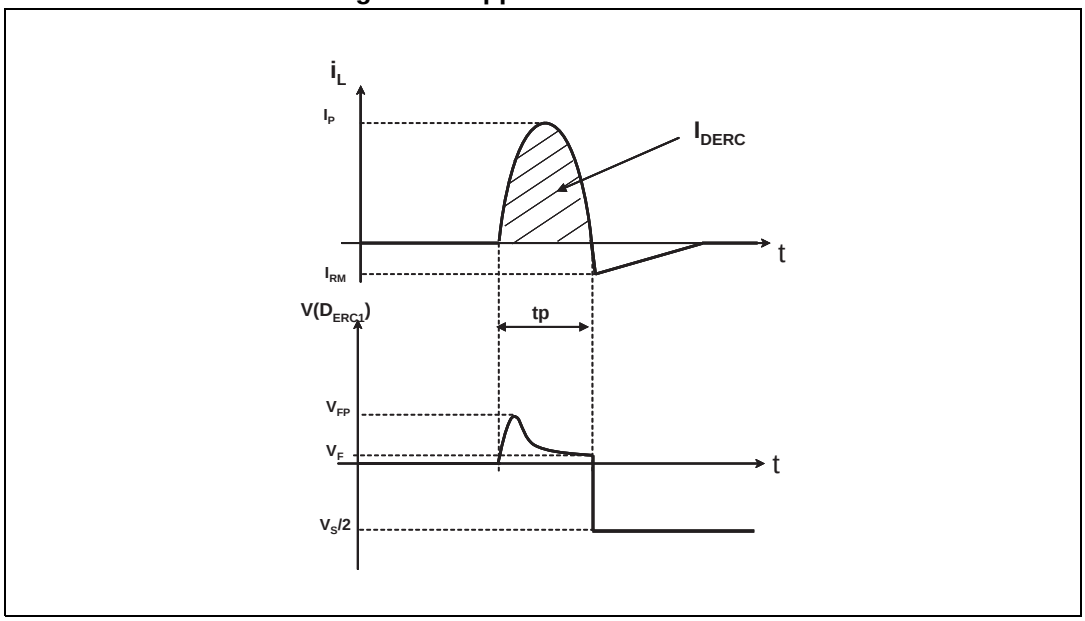


Figure 11. Application waveforms



3 Package information

- Epoxy meets UL94, V0
- Cooling method: by conduction (C)
- Recommended torque value: 0.5 N·m
- Maximum torque value: 1.0 N·m

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Figure 12. TO-247 dimension definitions

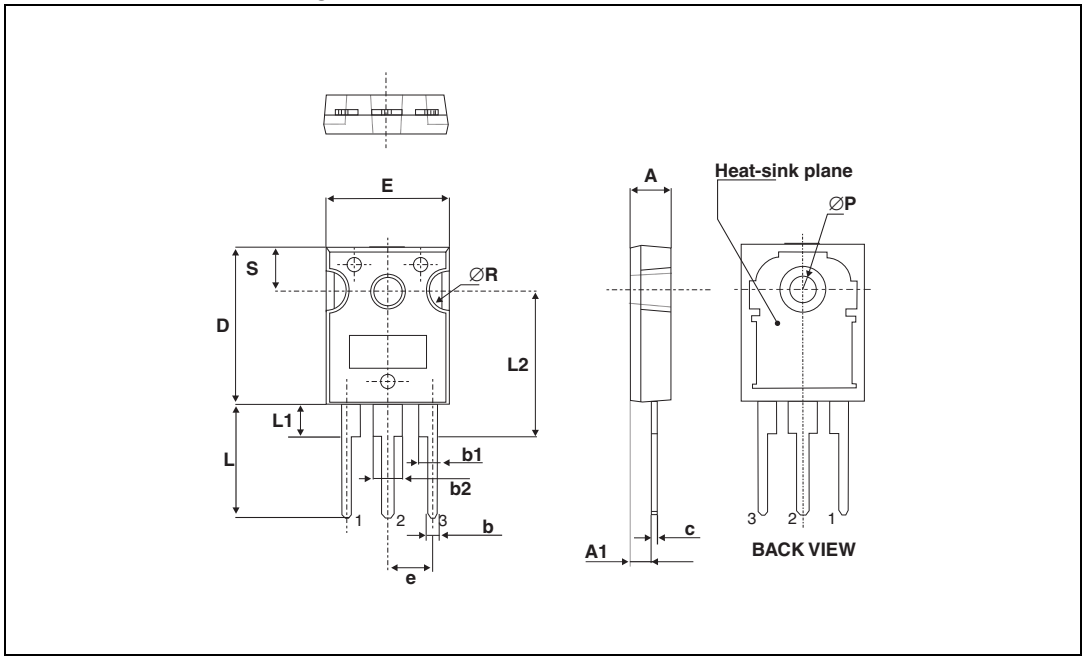

Table 6. TO-247 dimension values

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ	Max.
A	4.85		5.15	0.191		0.203
A1	2.20		2.60	0.086		0.102
b	1.00		1.40	0.039		0.055
b1	2.00		2.40	0.078		0.094
b2	3.00		3.40	0.118		0.133
c	0.40		0.80	0.015		0.031
D(1)	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e	5.30	5.45	5.60	0.209	0.215	0.220
L	14.20		14.80	0.559		0.582
L1	3.70		4.30	0.145		0.169
L2	18.50 typ.			0.728 typ.		
∅P(2)	3.55		3.65	0.139		0.143
∅R	4.50		5.50	0.177		0.217
S	5.30	5.50	5.70	0.209	0.216	0.224

1. Dimension D plus gate protrusion does not exceed 20.5 mm.
2. Resin thickness around the mounting hole is not less than 0.9 mm.

4 Ordering information

Table 7. Ordering information

Ordering type	Marking	Package	Weight	Base qty	Delivery mode
STTH60P03SW	STTH60P03SW	TO-247	4.46 g	30	Tube

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
04-Nov-2004	1	First issue.
10-Jan-2005	2	Minor layout update. No content change.
04-03-2005	3	Table 7 on page 5: base quantity delivery from 50 to 30.
19-Mar-2013	4	Added ECOPACK statement.

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SKM100GAL12T4

SEMITRANS® 2

Fast IGBT4 Modules

SKM100GAL12T4

Features

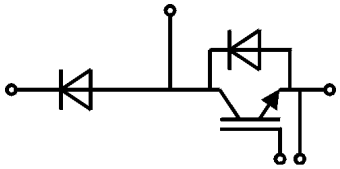
- IGBT4 = 4. generation fast trench IGBT (Infineon)
- CAL4 = Soft switching 4. generation CAL-diode
- Isolated copper baseplate using DBC technology (Direct Bonded Copper)
- Increased power cycling capability
- With integrated gate resistor
- For higher switching frequenzies up to 20kHz
- UL recognized, file no. E63532

Typical Applications*

- Electronic welders at fsw up to 20 kHz
- DC/DC – converter
- Brake chopper
- Switched reluctance motor

Remarks

- Case temperature limited to T_c = 125°C max.
- Recommended T_{op} = -40 ... +150°C
- Product reliability results valid for T_j = 150°C



GAL

Absolute Maximum Ratings

Symbol	Conditions		Values	Unit
IGBT				
V_{CES}	T_j = 25 °C		1200	V
I_C	T_j = 175 °C	T_c = 25 °C	160	A
		T_c = 80 °C	123	A
I_{Cnom}			100	A
I_{CRM}	I_{CRM} = 3xI_{Cnom}		300	A
V_{GES}			-20 ... 20	V
t_{psc}	V_{CC} = 800 V V_{GE} ≤ 15 V V_{CES} ≤ 1200 V	T_j = 150 °C	10	µs
T_j			-40 ... 175	°C
Inverse diode				
I_F	T_j = 175 °C	T_c = 25 °C	121	A
		T_c = 80 °C	91	A
I_{Fnom}			100	A
I_{FRM}	I_{FRM} = 3xI_{Fnom}		300	A
I_{FSM}	t_p = 10 ms, sin 180°, T_j = 25 °C		550	A
T_j			-40 ... 175	°C
Freewheeling diode				
I_F	T_j = 175 °C	T_c = 25 °C	121	A
		T_c = 80 °C	91	A
I_{Fnom}			100	A
I_{FRM}	I_{FRM} = 3xI_{Fnom}		300	A
I_{FSM}	t_p = 10 ms, sin 180°, T_j = 25 °C		550	A
T_j			-40 ... 175	°C
Module				
$I_{t(RMS)}$	$T_{terminal}$ = 80 °C		200	A
T_{stg}			-40 ... 125	°C
V_{isol}	AC sinus 50 Hz, t = 1 min		4000	V

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
IGBT						
$V_{CE(sat)}$	I_C = 100 A V_{GE} = 15 V chiplevel	T_j = 25 °C		1.80	2.05	V
		T_j = 150 °C		2.20	2.40	V
V_{CE0}	chiplevel	T_j = 25 °C		0.8	0.9	V
		T_j = 150 °C		0.7	0.8	V
r_{CE}	V_{GE} = 15 V chiplevel	T_j = 25 °C		10.00	11.50	mΩ
		T_j = 150 °C		15.00	16.00	mΩ
$V_{GE(th)}$	V_{GE}=V_{CE}, I_C = 3.8 mA		5	5.8	6.5	V
I_{CES}	V_{GE} = 0 V V_{CE} = 1200 V	T_j = 25 °C			1	mA
		T_j = 150 °C				mA
C_{ies}	V_{CE} = 25 V V_{GE} = 0 V	f = 1 MHz		6.15		nF
C_{oes}		f = 1 MHz		0.40		nF
C_{res}		f = 1 MHz		0.345		nF
Q_G	V_{GE} = - 8 V...+ 15 V			565		nC
R_{Gint}	T_j = 25 °C			7.5		Ω

SKM100GAL12T4

SEMITRANS® 2

Fast IGBT4 Modules

SKM100GAL12T4

Features

- IGBT4 = 4. generation fast trench IGBT (Infineon)
- CAL4 = Soft switching 4. generation CAL-diode
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- Increased power cycling capability
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- UL recognized, file no. E63532

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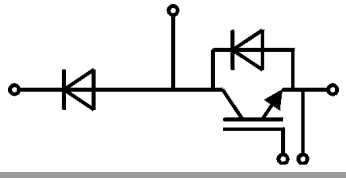
- DC/DC – converter
- Brake chopper
- Switched reluctance motor

Remarks

- Case temperature limited to T_c = 125°C max.
- Recommended T_{op} = -40 ... +150°C
- Product reliability results valid for T_j = 150°C

Characteristics

Symbol	Conditions		min.	typ.	max.	Unit
$t_{d(on)}$	V_{CC} = 600 V I_C = 100 A V_{GE} = ±15 V $R_{G\ on}$ = 1 Ω $R_{G\ off}$ = 1 Ω di/dt_{on} = 1800 A/µs di/dt_{off} = 1130 A/µs	T_j = 150 °C		165		ns
t_r		T_j = 150 °C		47		ns
E_{on}		T_j = 150 °C		15		mJ
$t_{d(off)}$		T_j = 150 °C		400		ns
t_f		T_j = 150 °C		75		ns
E_{off}		T_j = 150 °C		10.2		mJ
$R_{th(j-c)}$	per IGBT				0.27	K/W
Inverse diode						
$V_F = V_{EC}$	I_F = 100 A V_{GE} = 0 V chiplevel	T_j = 25 °C		2.20	2.52	V
		T_j = 150 °C		2.15	2.47	V
V_{F0}	chiplevel	T_j = 25 °C		1.3	1.5	V
		T_j = 150 °C		0.9	1.1	V
r_F	chiplevel	T_j = 25 °C		9.0	10.2	mΩ
		T_j = 150 °C		12.5	13.7	mΩ
I_{RRM}	I_F = 100 A di/dt_{off} = 1600 A/µs V_{GE} = ±15 V V_{CC} = 600 V	T_j = 150 °C		54		A
Q_{rr}		T_j = 150 °C		15.7		µC
E_{rr}		T_j = 150 °C		5.9		mJ
$R_{th(j-c)}$	per diode				0.48	K/W
Freewheeling diode						
$V_F = V_{EC}$	I_F = 100 A V_{GE} = 0 V chiplevel	T_j = 25 °C		2.20	2.52	V
		T_j = 150 °C		2.15	2.47	V
V_{F0}	chiplevel	T_j = 25 °C		1.3	1.5	V
		T_j = 150 °C		0.9	1.1	V
r_F	chiplevel	T_j = 25 °C		9.0	10.2	mΩ
		T_j = 150 °C		12.5	13.7	mΩ
I_{RRM}	I_F = 100 A di/dt_{off} = 1600 A/µs V_{GE} = ±15 V V_{CC} = 600 V	T_j = 150 °C		54		A
Q_{rr}		T_j = 150 °C		15.7		µC
E_{rr}		T_j = 150 °C		5.9		mJ
$R_{th(j-c)}$	per Diode				0.48	K/W
Module						
L_{CE}					30	nH
$R_{CC'+EE'}$	terminal-chip	T_C = 25 °C		0.65		mΩ
		T_C = 125 °C		1		mΩ
$R_{th(c-s)}$	per module			0.04	0.05	K/W
M_s	to heat sink M6		3		5	Nm
M_t		to terminals M5	2.5		5	Nm
						Nm
w					160	g



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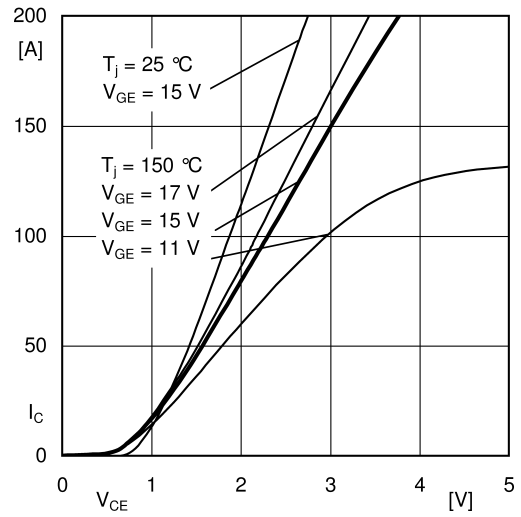


Fig. 1: Typ. output characteristic, inclusive $R_{CC'+EE'}$

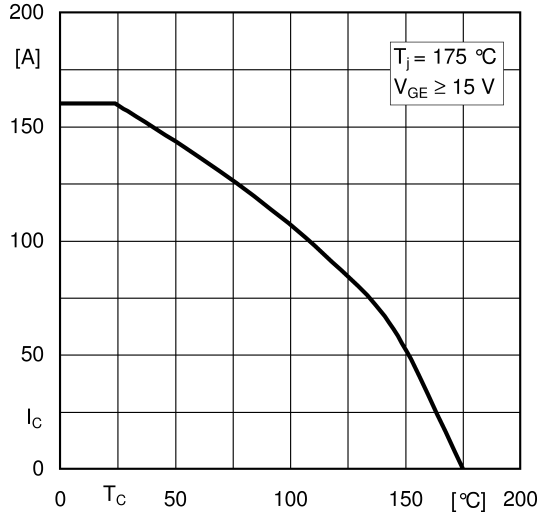


Fig. 2: Rated current vs. temperature $I_C = f(T_C)$

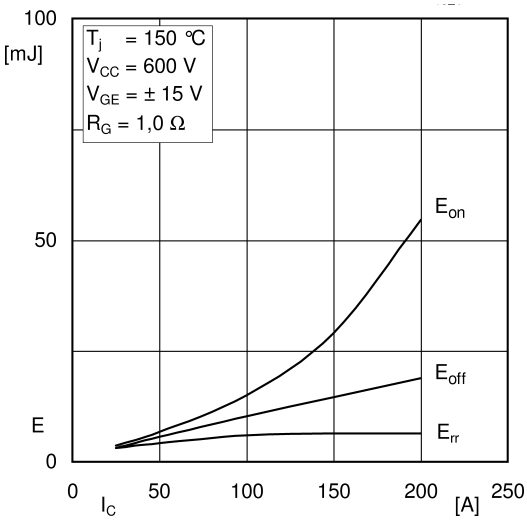


Fig. 3: Typ. turn-on /-off energy = f (I_C)

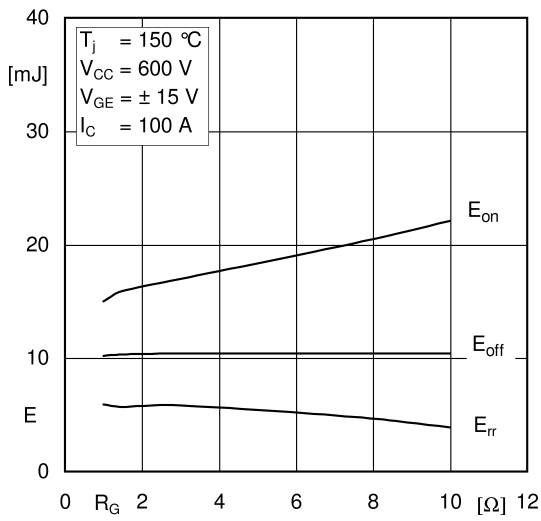


Fig. 4: Typ. turn-on /-off energy = f (R_G)

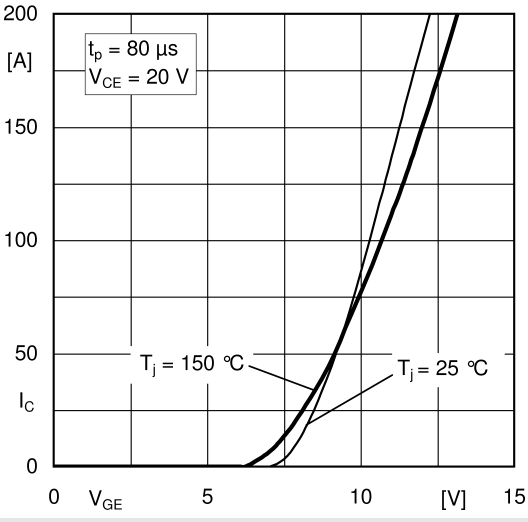


Fig. 5: Typ. transfer characteristic

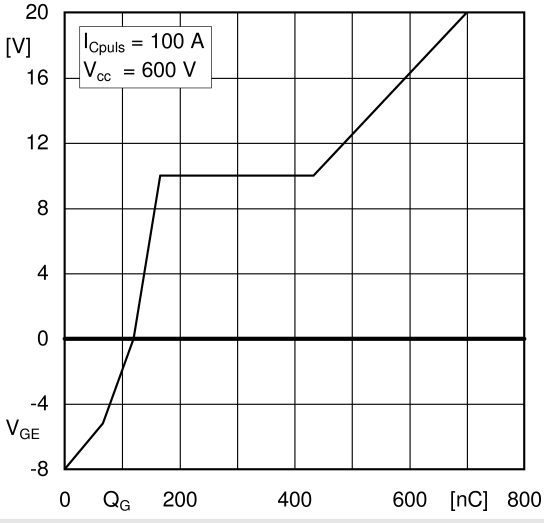


Fig. 6: Typ. gate charge characteristic

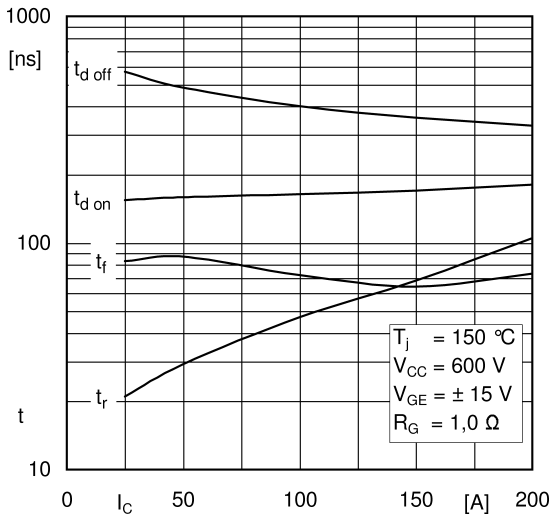


Fig. 7: Typ. switching times vs. I_C

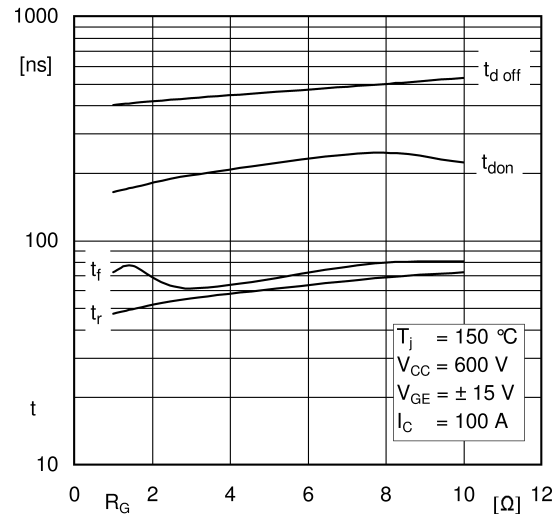


Fig. 8: Typ. switching times vs. gate resistor R_G

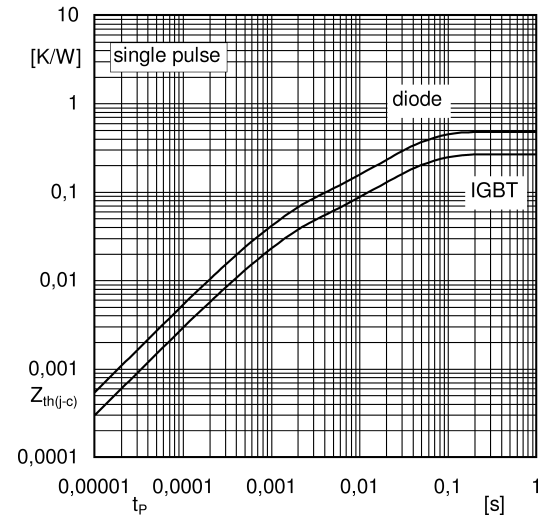


Fig. 9: Transient thermal impedance

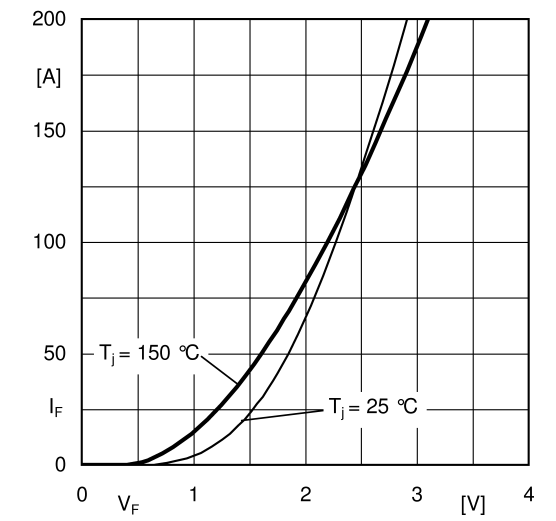


Fig. 10: Typ. CAL diode forward charact., incl. $R_{CC'+EE'}$

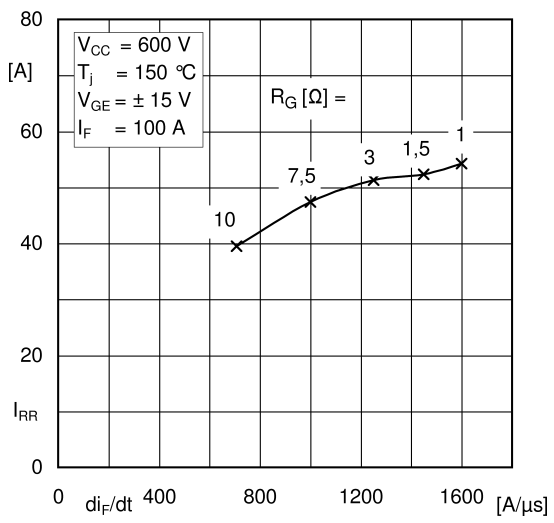


Fig. 11: CAL diode peak reverse recovery current

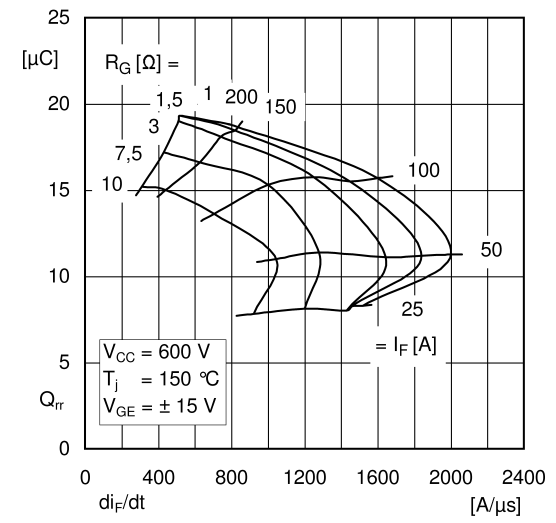
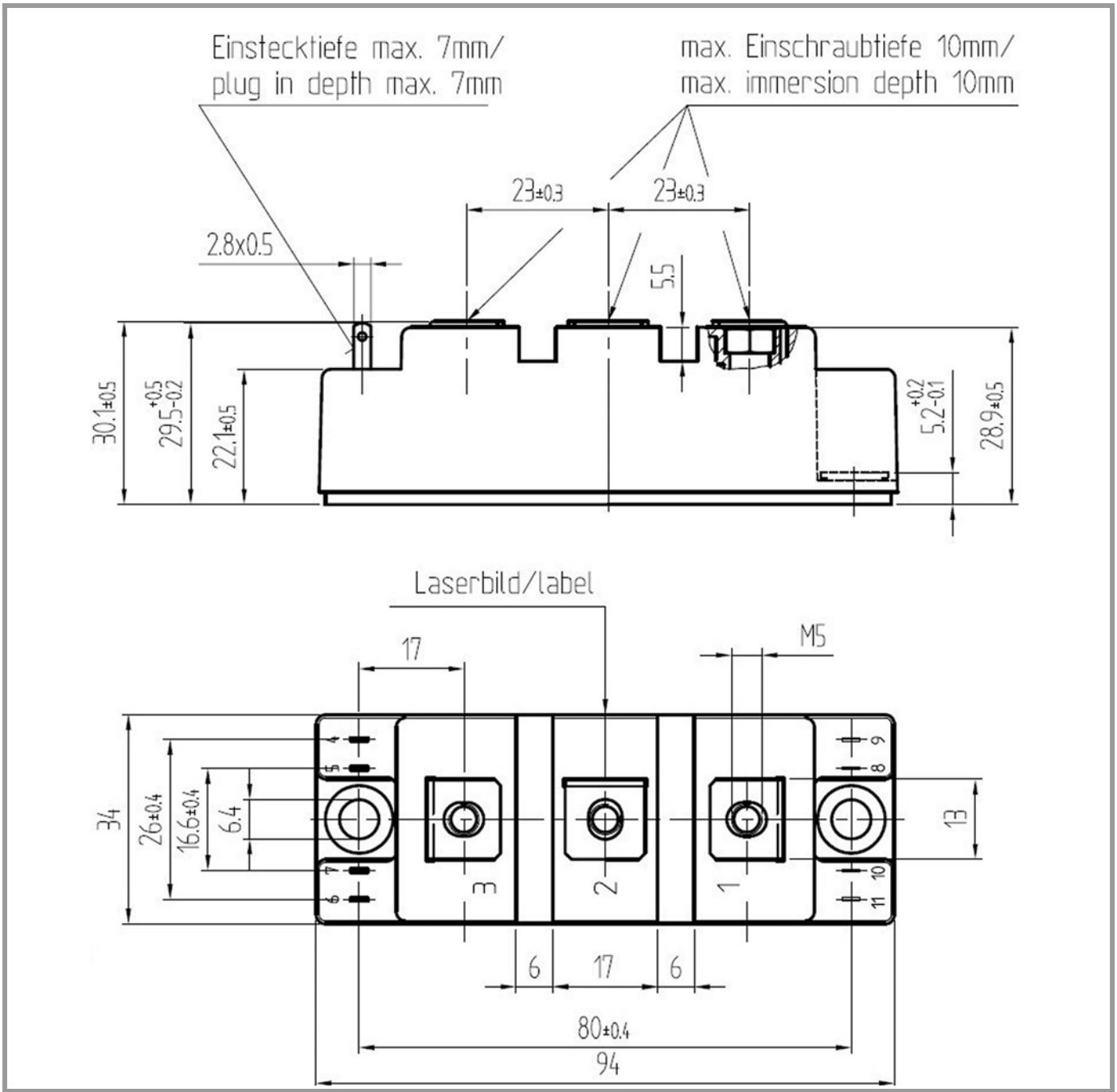


Fig. 12: Typ. CAL diode peak reverse recovery charge



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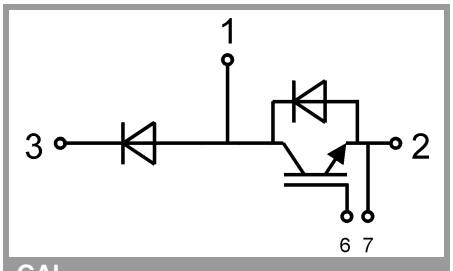


GAL

This is an electrostatic discharge sensitive device (ESDS), international standard IEC 60747-1, Chapter IX

* The specifications of our components may not be considered as an assurance of component characteristics. Components have to be tested for the respective application. Adjustments may be necessary. The use of SEMIKRON products in life support appliances and systems is subject to prior specification and written approval by SEMIKRON. We therefore strongly recommend prior consultation of our staff.

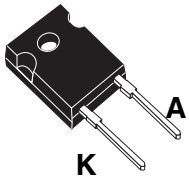
A.7

STTH6012

Ultrafast recovery - 1200 V diode

Main product characteristics

$I_{F(AV)}$	60 A
V_{RRM}	1200 V
T_j	175° C
V_F (typ)	1.30 V
t_{rr} (typ)	50 ns



DO-247
STTH6012W

Features and benefits

- Ultrafast, soft recovery
- Very low conduction and switching losses
- High frequency and/or high pulsed current operation
- High reverse voltage capability
- High junction temperature

Description

The high quality design of this diode has produced a device with low leakage current, regularly reproducible characteristics and intrinsic ruggedness. These characteristics make it ideal for heavy duty applications that demand long term reliability.

Such demanding applications include industrial power supplies, motor control, and similar mission-critical systems that require rectification and freewheeling. These diodes also fit into auxiliary functions such as snubber, bootstrap, and demagnetization applications.

The improved performance in low leakage current, and therefore thermal runaway guard band, is an immediate competitive advantage for this device.

Order codes

Part Number	Marking
STTH6012W	STTH6012W

1 Characteristics

Table 1. Absolute ratings (limiting values at 25° C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		1200	V
$I_{F(RMS)}$	RMS forward current		80	A
$I_{F(AV)}$	Average forward current, $\delta = 0.5$	T_c = 90° C	60	A
I_{FRM}	Repetitive peak forward current	t_p = 5 µs, F = 5 kHz square	500	A
I_{FSM}	Surge non repetitive forward current	t_p = 10 ms Sinusoidal	400	A
T_{stg}	Storage temperature range		-65 to + 175	°C
T_j	Maximum operating junction temperature		175	°C

Table 2. Thermal parameter

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	Junction to case	0.6	°C/W

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ	Max.	Unit
I_R(1)	Reverse leakage current	T_j = 25° C	$V_R = V_{RRM}$			30	µA
		T_j = 125° C			30	300	
V_F(2)	Forward voltage drop	T_j = 25° C	I_F = 60 A			2.25	V
		T_j = 125° C			1.35	2.05	
		T_j = 150° C			1.30	1.95	

1. Pulse test: t_p = 5 ms, δ < 2 %
2. Pulse test: t_p = 380 µs, δ < 2 %

To evaluate the conduction losses use the following equation:
$P = 1.50 \times I_{F(AV)} + 0.0075\ I_F{}^2{}_{(RMS)}$

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ	Max.	Unit
t_{rr}	Reverse recovery time	I_F = 1 A, dI_F/dt = -50 A/µs, V_R = 30 V, T_j = 25° C			125	ns
		I_F = 1 A, dI_F/dt = -100 A/µs, V_R = 30 V, T_j = 25° C		63	85	
		I_F = 1 A, dI_F/dt = -200 A/µs, V_R = 30 V, T_j = 25° C		50	70	
I_{RM}	Reverse recovery current	I_F = 60 A, dI_F/dt = -200 A/µs, V_R = 600 V, T_j = 125° C		32	45	A
S	Softness factor	I_F = 60 A, dI_F/dt = -200 A/µs, V_R = 600 V, T_j = 125° C		1		
t_{fr}	Forward recovery time	I_F = 60 A dI_F/dt = 100 A/µs V_{FR} = 1.5 x V_{Fmax}, T_j = 25° C			750	ns
V_{FP}	Forward recovery voltage	I_F = 60 A, dI_F/dt = 100 A/µs, T_j = 25° C		4.5		V

Figure 1. Conduction losses versus average current

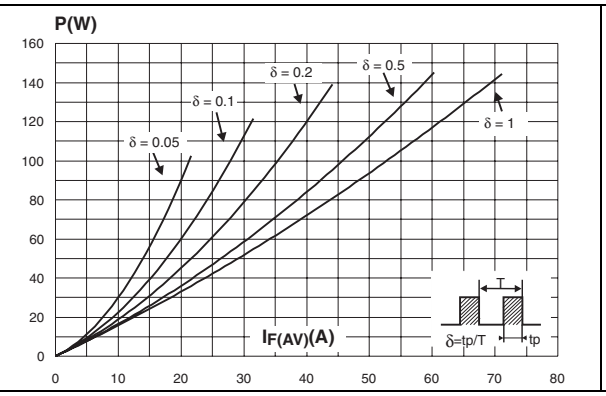


Figure 2. Forward voltage drop versus forward current

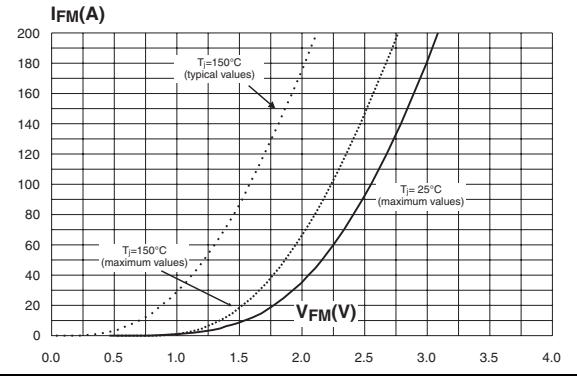


Figure 3. Relative variation of thermal impedance junction to case versus pulse duration

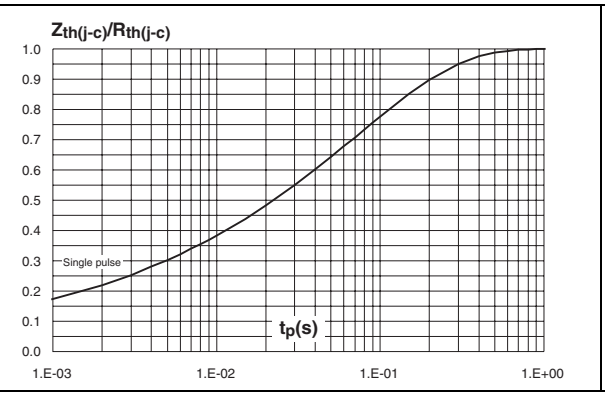


Figure 4. Peak reverse recovery current versus dI_F/dt (typical values)

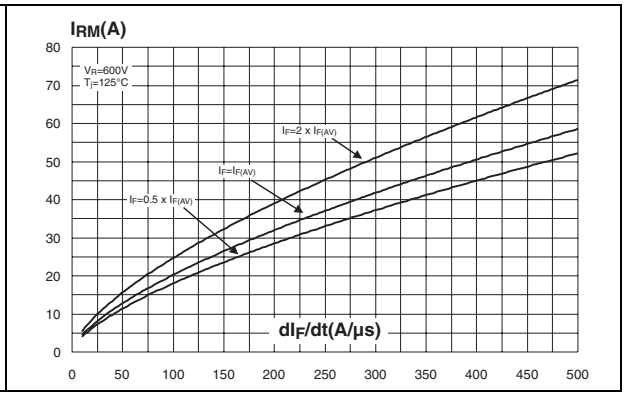


Figure 5. Reverse recovery time versus dI_F/dt (typical values)

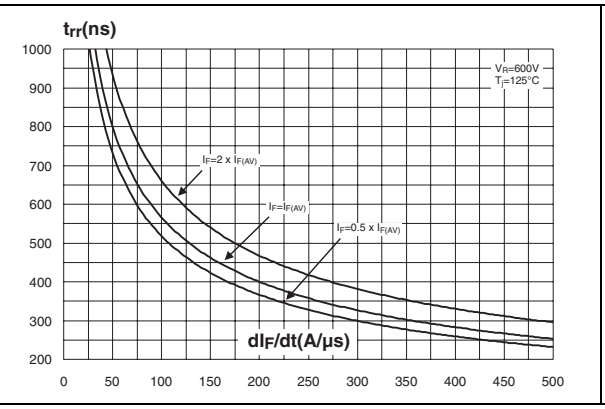


Figure 6. Reverse recovery charges versus dI_F/dt (typical values)

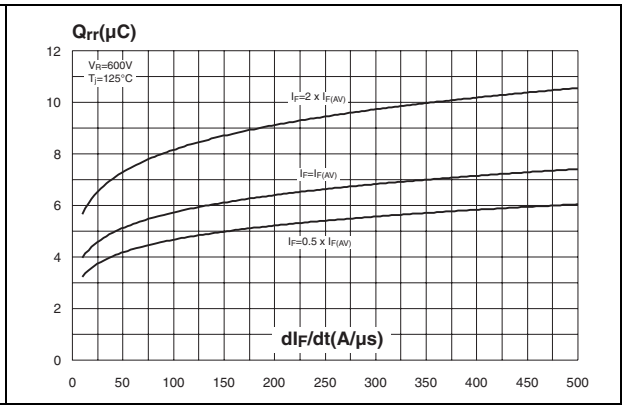


Figure 7. Softness factor versus dI_F/dt (typical values)

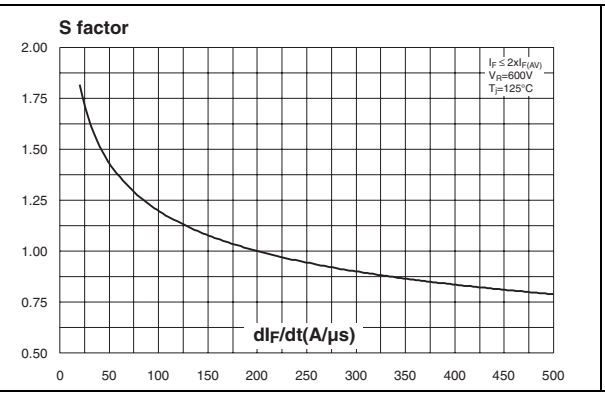


Figure 8. Relative variations of dynamic parameters versus junction temperature

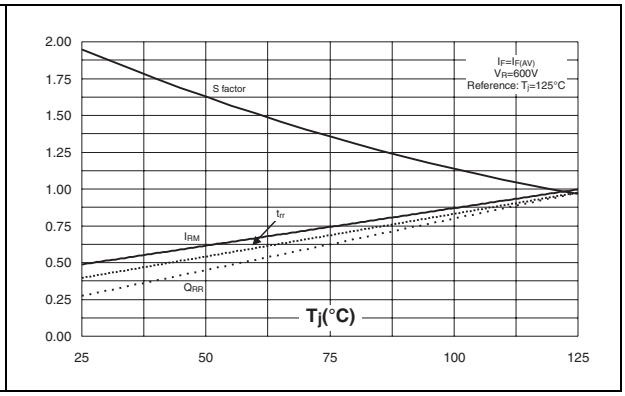


Figure 9. Transient peak forward voltage versus dI_F/dt (typical values)

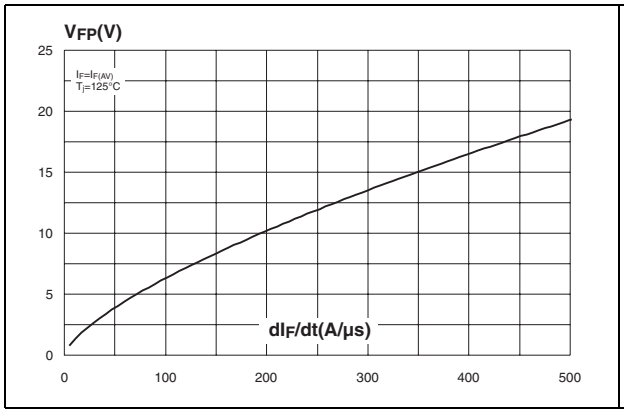


Figure 10. Forward recovery time versus dI_F/dt (typical values)

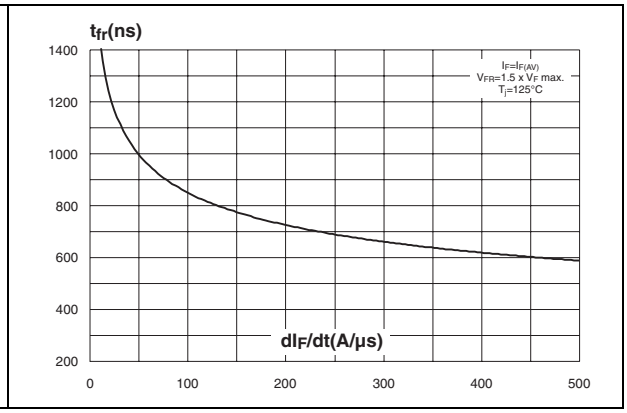
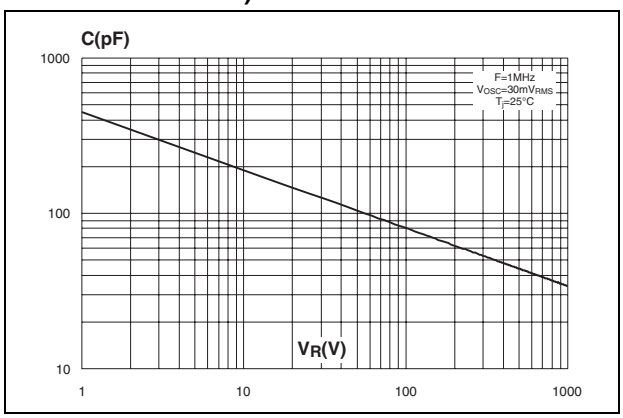


Figure 11. Junction capacitance versus reverse voltage applied (typical values)



2 Package information

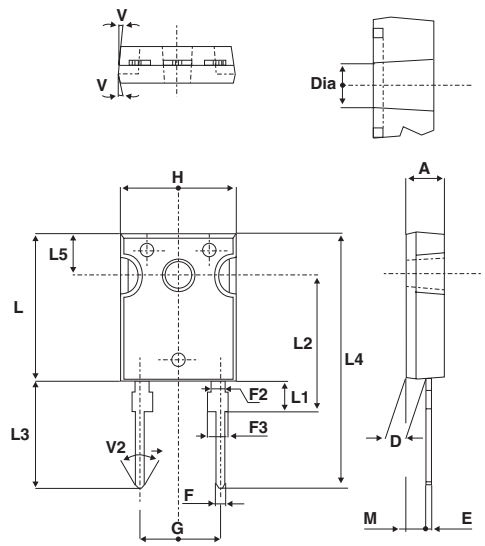
Epoxy meets UL94, V0

Cooling method: by conduction (C)

Recommended torque value: 0.80 Nm

Maximum torque value: 1.0 Nm

Table 5. DO-247 dimensions



REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.		Max	Min.		Max.
A	4.85		5.15	0.191		0.203
D	2.20		2.60	0.086		0.102
E	0.40		0.80	0.015		0.031
F	1.00		1.40	0.039		0.055
F2		2.00			0.078	
F3	2.00		2.40	0.078		0.094
G		10.90			0.429	
H	15.45		15.75	0.608		0.620
L	19.85		20.15	0.781		0.793
L1	3.70		4.30	0.145		0.169
L2		18.50			0.728	
L3	14.20		14.80	0.559		0.582
L4		34.60			1.362	
L5		5.50			0.216	
M	2.00		3.00	0.078		0.118
V		5°			5°	
V2		60°			60°	
Dia.	3.55		3.65	0.139		0.143

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

3 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
STTH6012W	STTH6012W	DO-247	4.4 g	30	Tube

4 Revision history

Date	Revision	Description of Changes
02-Mar-2006	1	First issue.